Charge and Light Sensing in Noble Liquid TPCs

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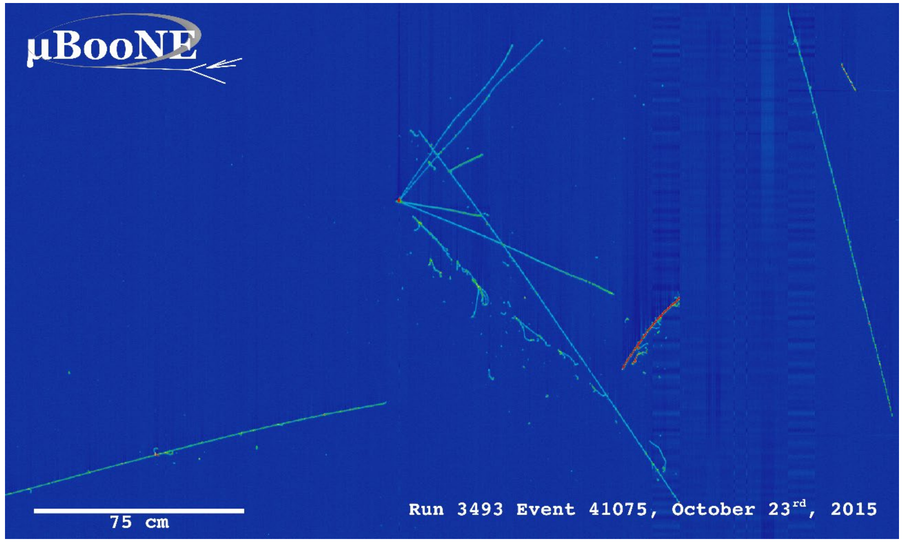
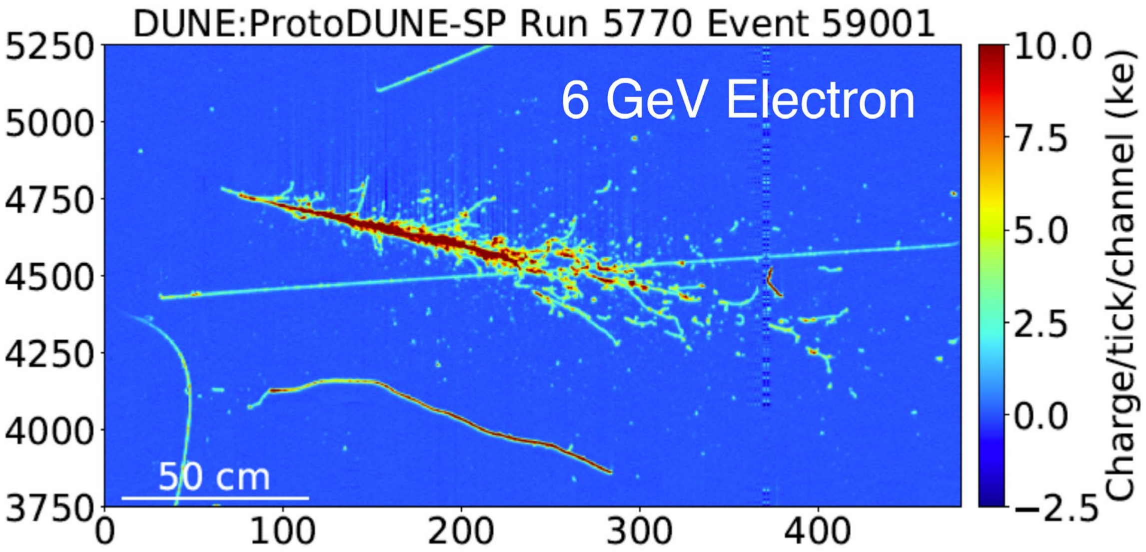
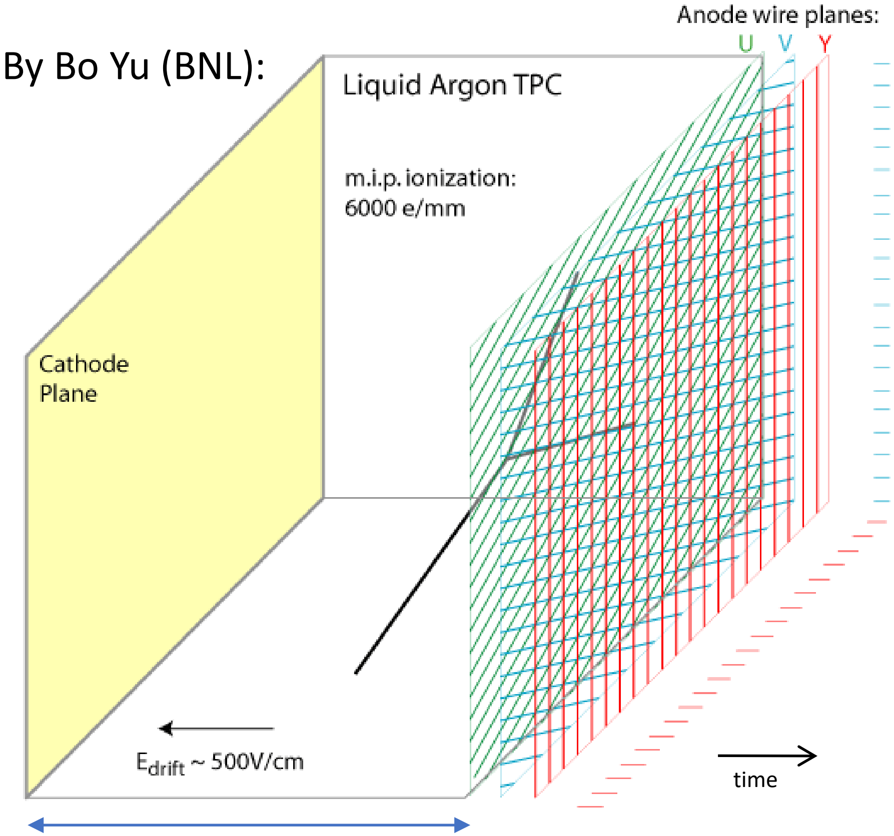
Principle of Liquid Argon Time Projection Chamber (LArTPC)

- ~mm scale position resolution with multiple 1D wire/strip/pad readouts





By Bo Yu (BNL):



1.5, 2.5, 3.6 m (6m?)

Drift velocity 1.6 m/ms → ms drift time

Signal Formation: Induced Signals from a Track Segment

Waveform calculation: Bo Yu

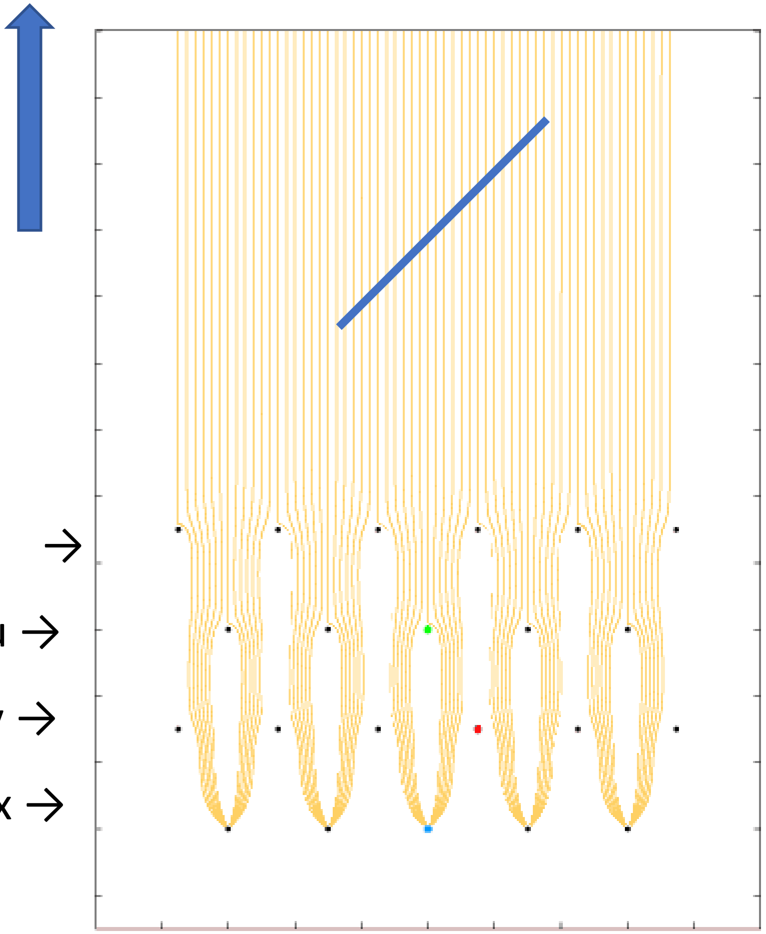
Cathode
3.6 meters away
in pDUNE
(up to 6 m in
DUNE FD-2)

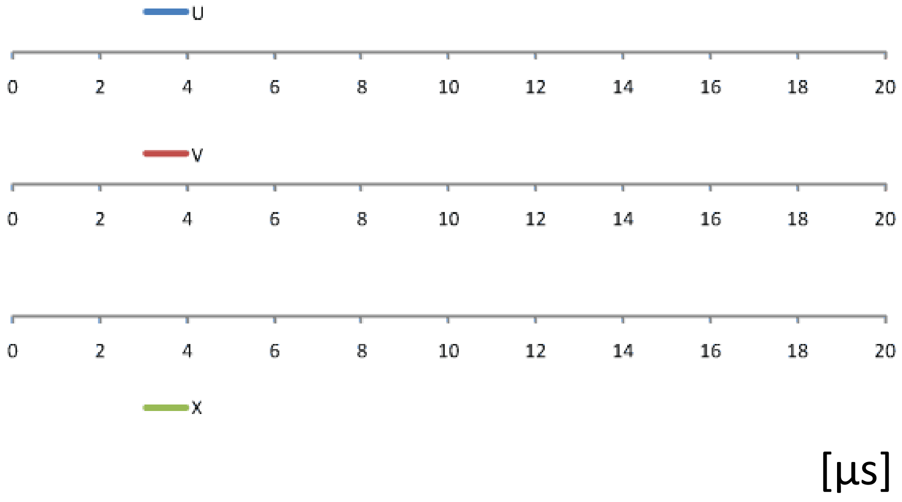
Grid ! →

Induction plane u →

Induction plane v →

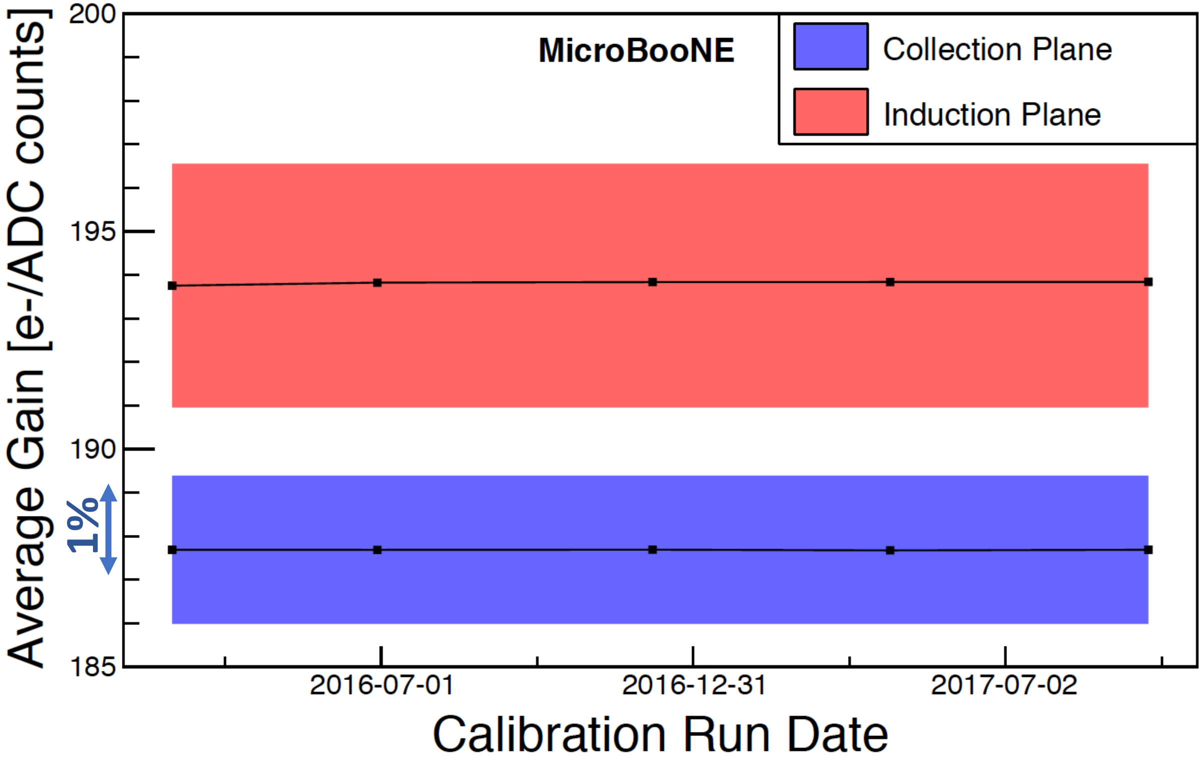
Collection plane x →



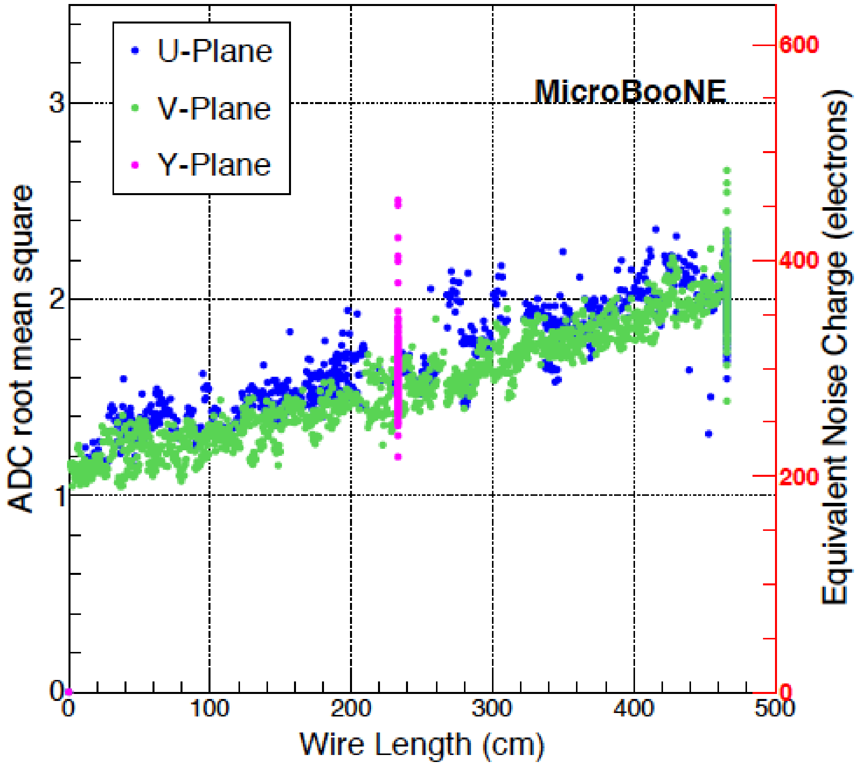


ProtoDUNE style wire arrangement: **3 instrumented wire planes (u, v, y) + 1 grid plane**
Raw current waveforms convolved with a 0.5 µs gaussian (~1/2 drift length) to mimic diffusion

Stability and Performance of LAr TPCs with Cold Electronics



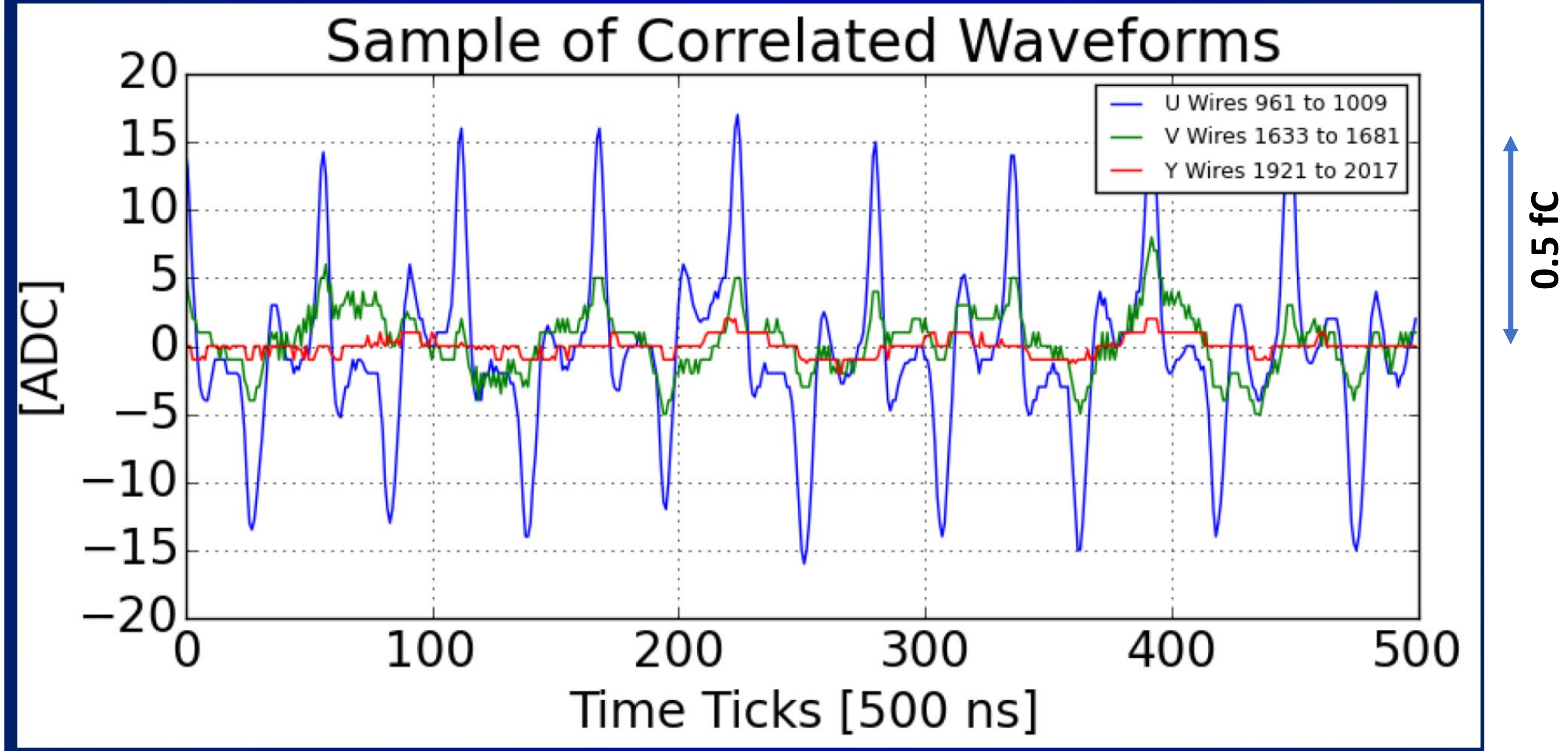
Wire Noise Level in MicroBooNE



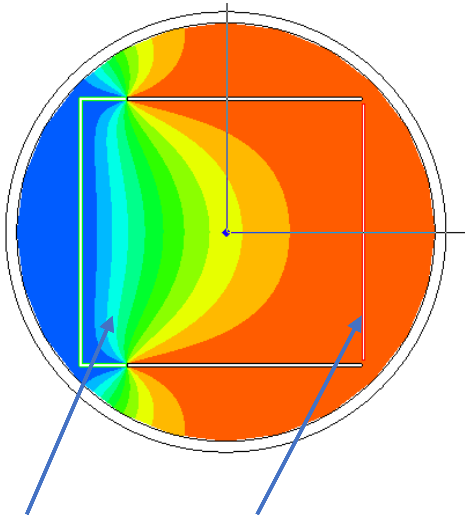
- Electronic calibration
  - Cold electronics gain in **MicroBooNE** stable over two year period, ***variation <0.2%.*** **(Stable over ~7 years …)**; in ProtoDUNE, stable over 2 years (operation time).
- Excellent noise performance in MB and ProtoDUNE
  - MB: ENC after ***excess noise*** filtering is < **400 e^-** for 85% of channels (~7000 wires)
  - **ProtoDUNE**: SNR measured by cosmic muons: **Collection: 48.7:1, Induction: 21.2:1**

Excess noise in MB from cathode 2.5 m away with HV= 70 kV

HV ripple (36 kHz fundamental) induced on sense wires (no grid)



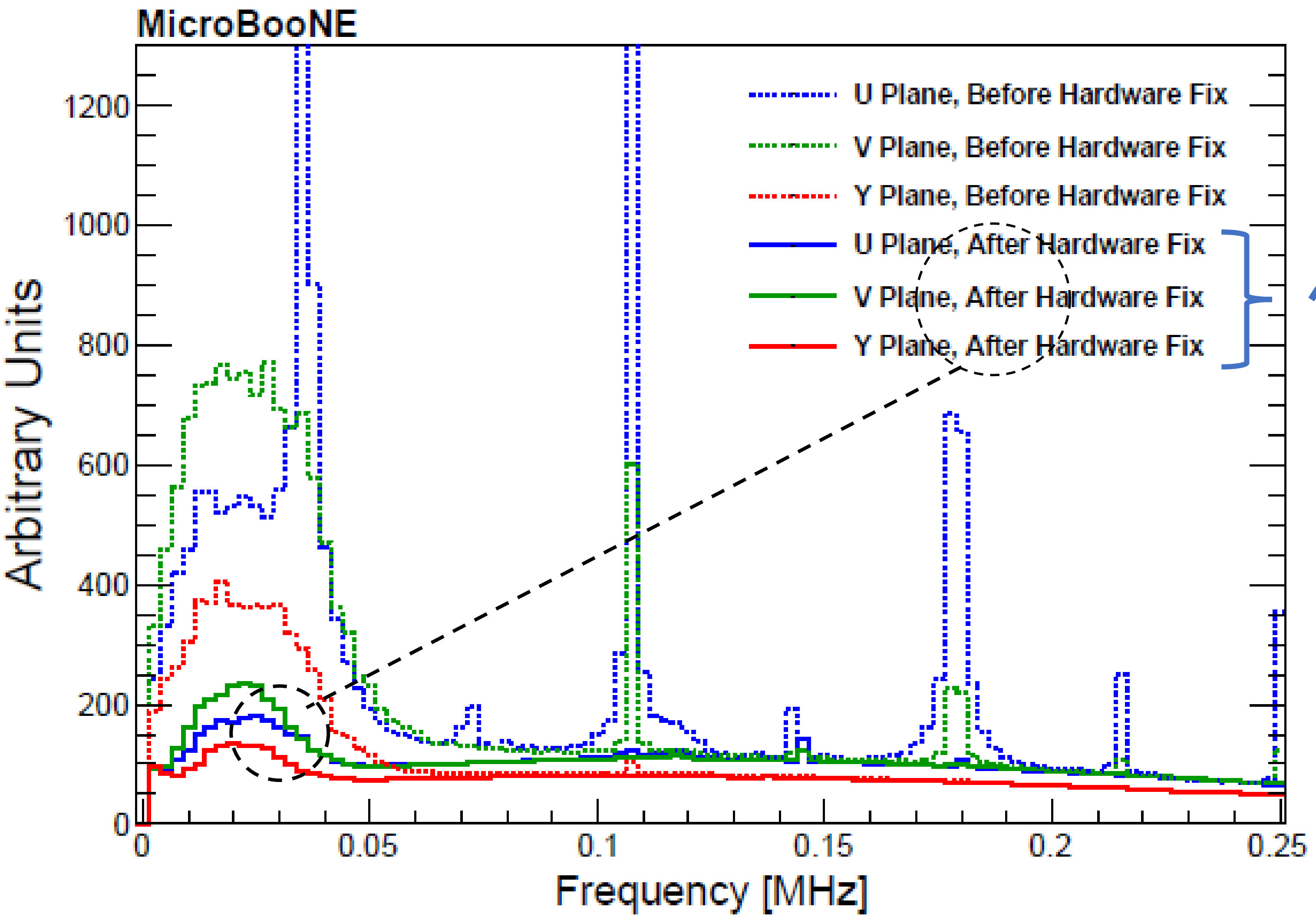
Noise induced by the cathode is progressively attenuated by the shielding effect of the wire planes



Cathode-anode coupling ~ 1 pF/m^2 ~ **20 fF/wire in the 1st wire plane**

Cathode HV ripple must be less than **1 part in 10^7!**

Excess noise removal took some work …. Better HV filters



JINST 12 P08003 (2017)

nEXO “5 ton” LXe TPC – search for neutrinoless 2β decay

- ^{136}**Xe** is used both as the ***source and detection medium***.

Charge: **Q_0=16fC (10^5e)** from ***0νββ***

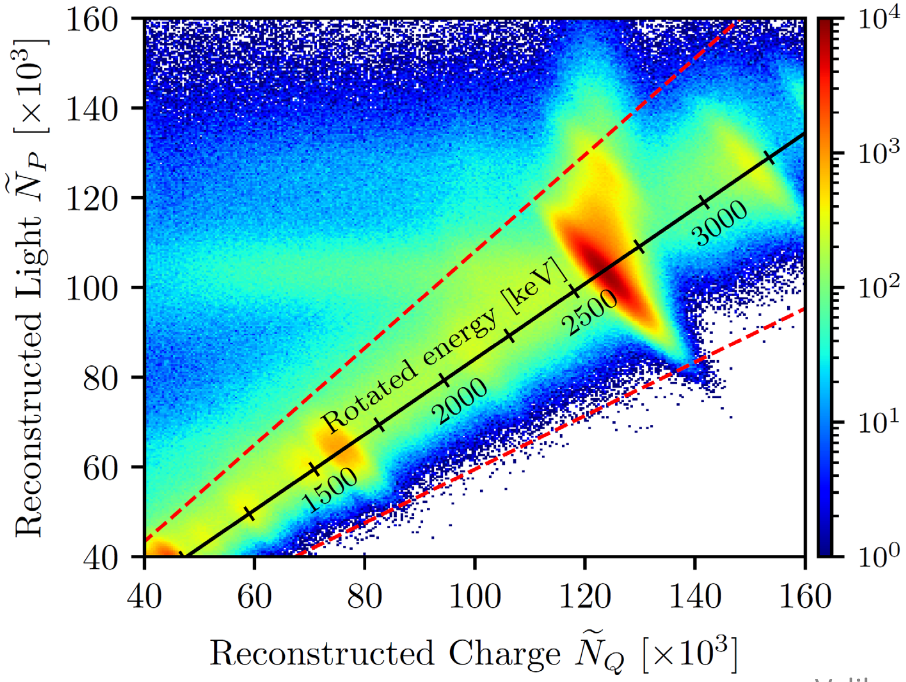
Charge from *0νββ* localized to a few *mm vs* wider spread background events

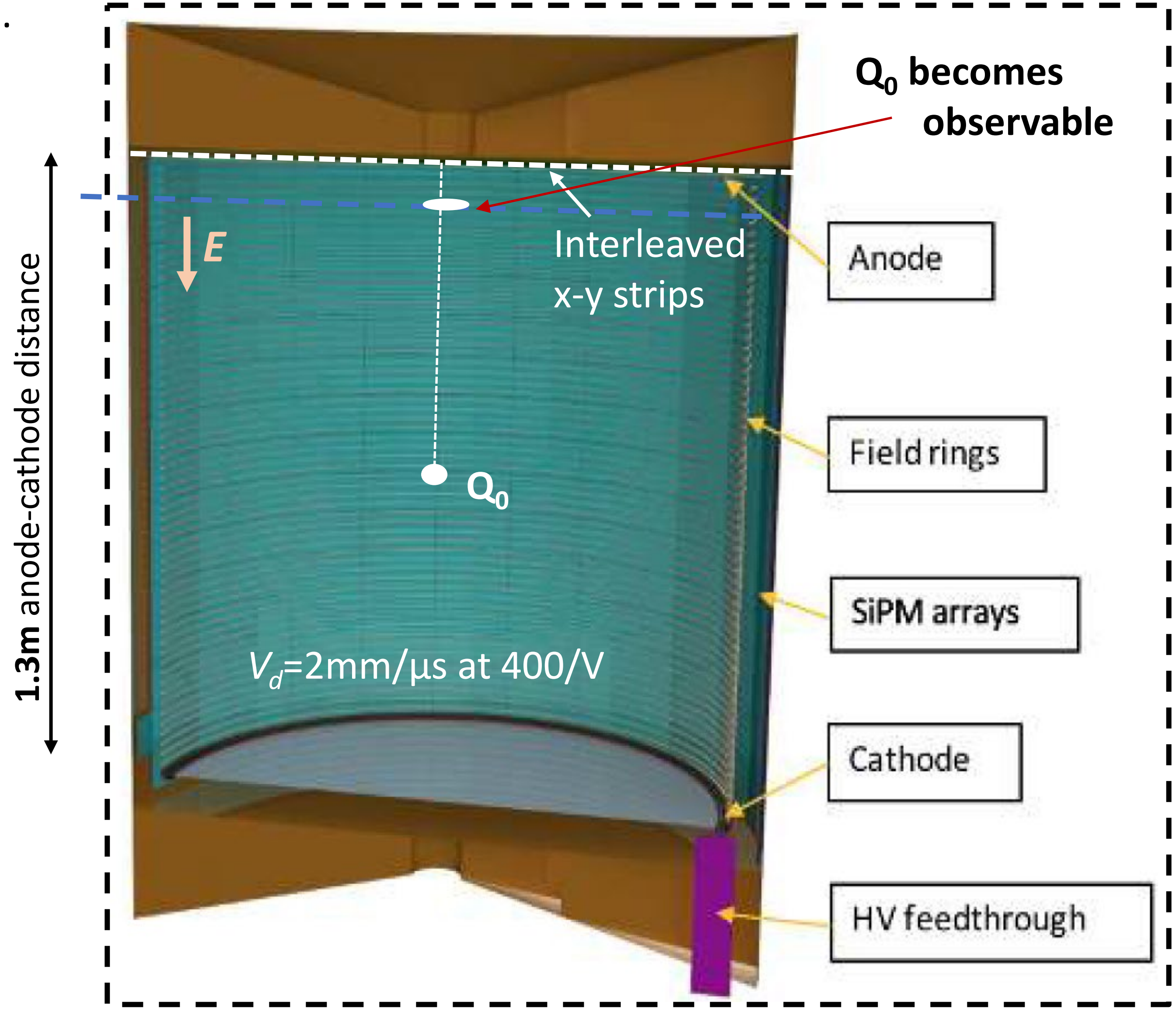
Sensing electrodes: single plane, interleaved x-y strips

Integration time: **~ 20μs (long induced signals)**;

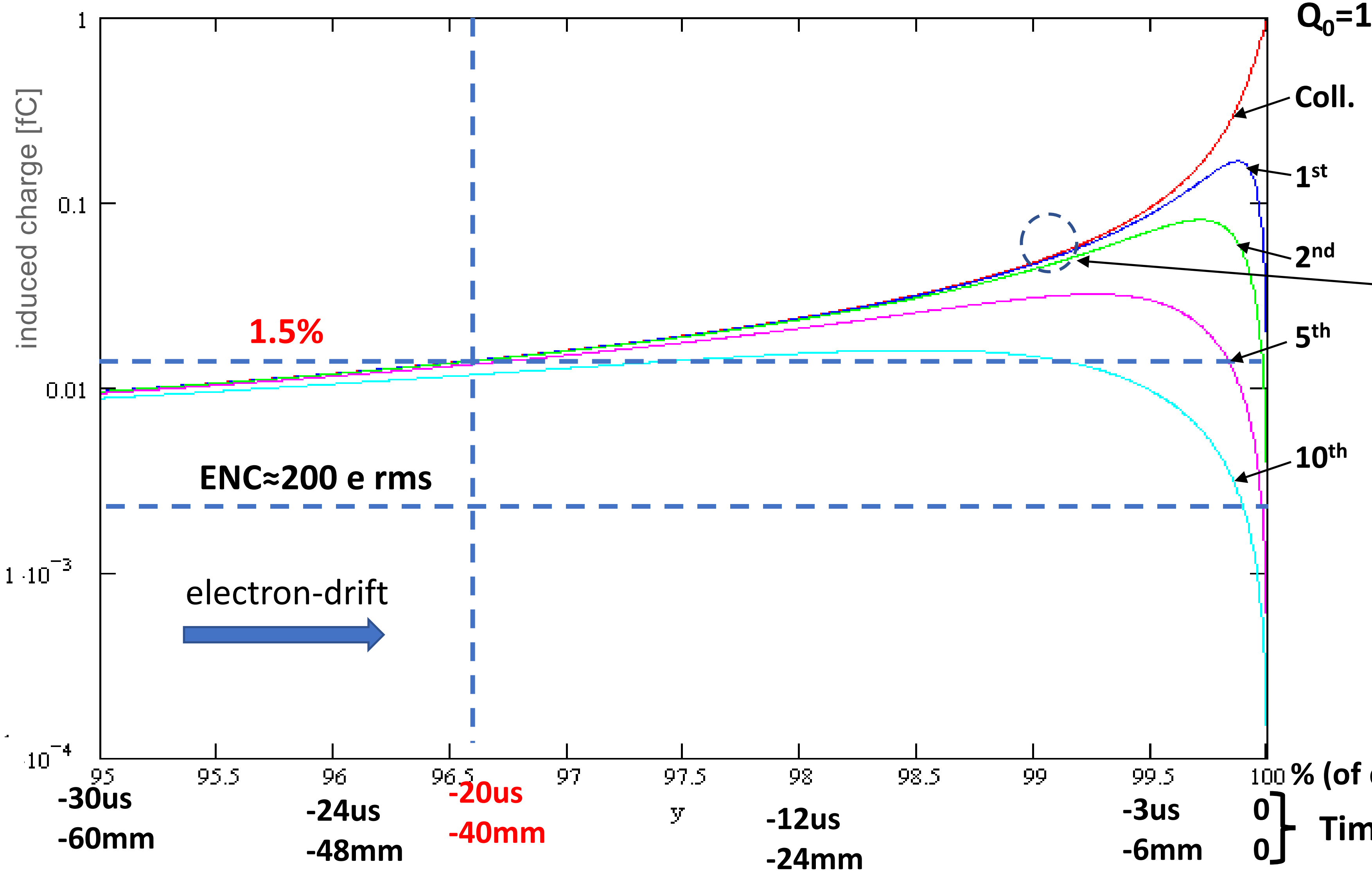
ENC~200 e rms, demonstrated by LAr cold electronics

Light: ~ **10^5 photons at 400 V/cm** from ***0νββ***





nEXO TPC: Charge induced on the collection strip and on 1st , 2nd , 5th , and 10th neighbor as a function of time and distance to the anode; 3mm strip pitch shown



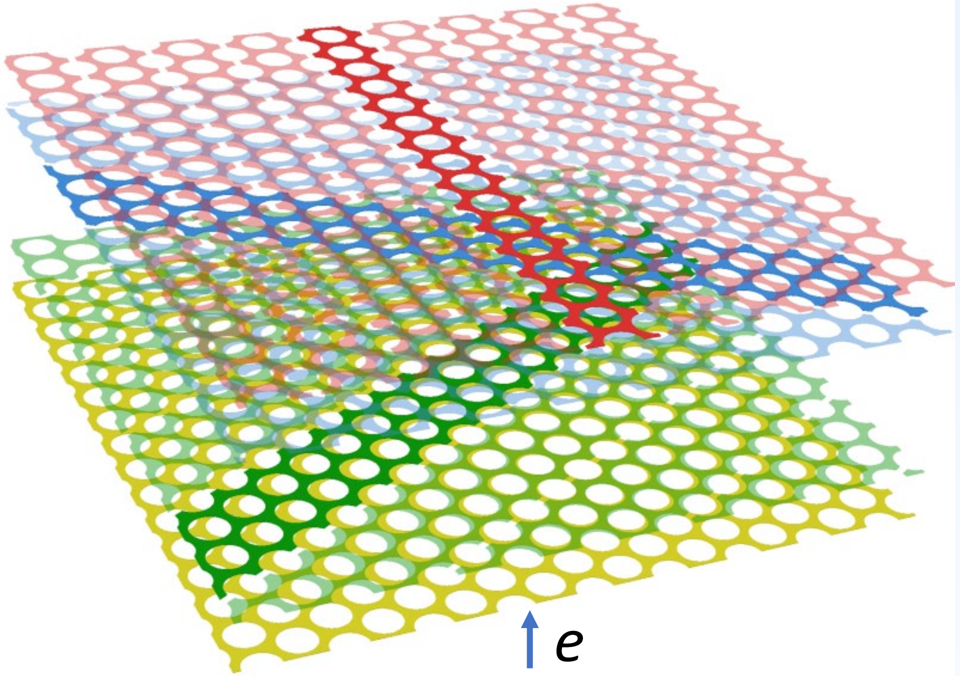
Q_0/ENC≈500

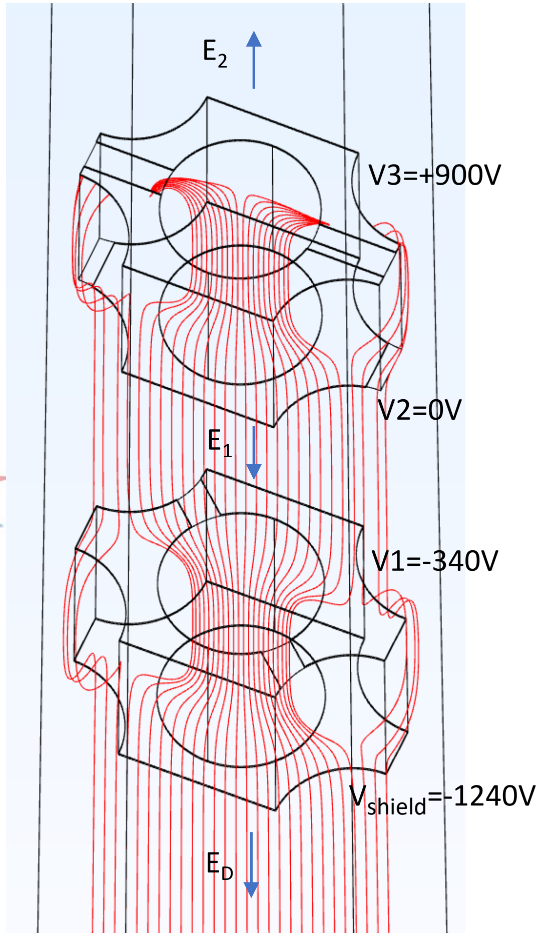
Equal charge induced on adjacent strips until ~1cm from the anode

Ballistic deficit:
1.5% at ~20 μs
1% at ~30 μs
Integration time could be reduced to 10 μs by a 2d grid – a separate study.

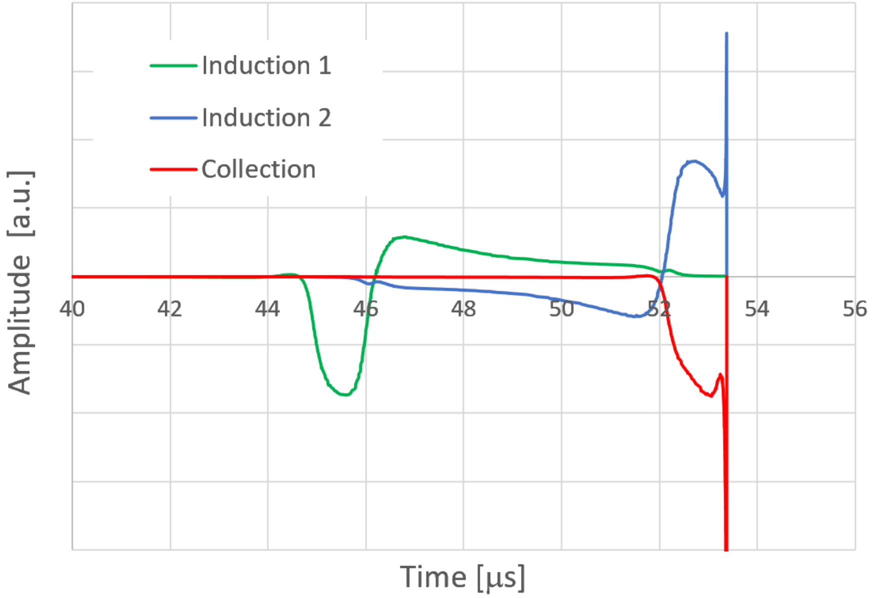
What is *new* for LAr DUNE-FD2 : A 3-View Perforated PCB Anode Readout Concept

A 3-view (+/-30°, 90°) strip readout. The substrate of the two PCBs are removed for clarity. One strip from each readout plane is highlighted.





Induced current waveforms from a strip in each view for a point charge passing through the middle of each strip.



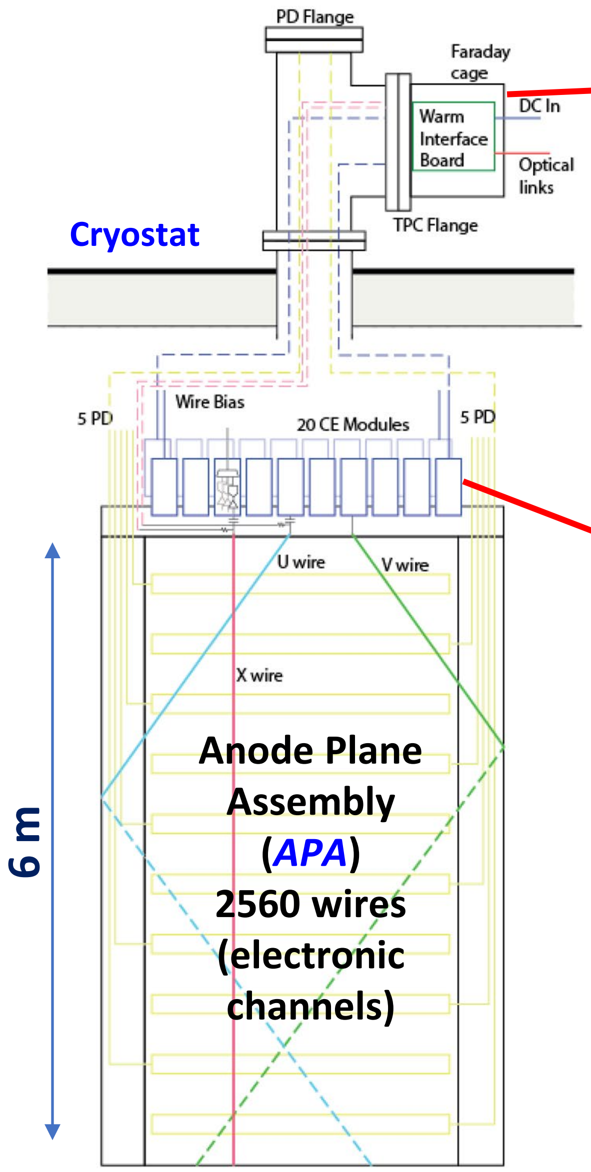
The first plane ("grid") facing the drift volume is not segmented, it is used for shielding the readout strips from charge injection from the cathode.

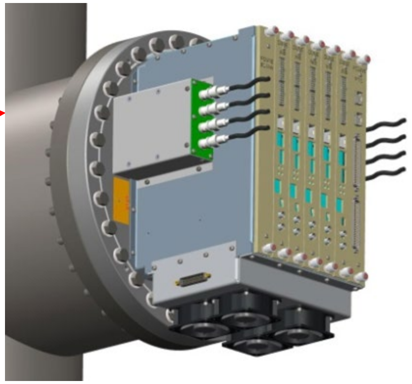
Typical PCB thickness: ~3mm
PCB separation: ~1cm
Hole size: 2-3mm

With proper bias voltage on each plane, ionization electrons can be pulled through multiple planes (induction views) without loss and be collected on the last one (collection view).

Concept developed by **F. Pietropaolo (CERN) and B. Yu (BNL)**

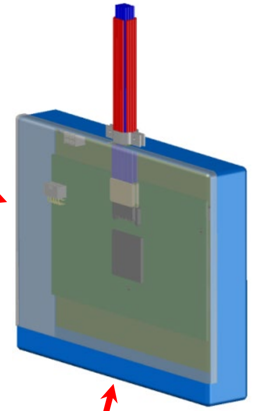
A Key to TPCs: Integral Faraday Cage and Readout

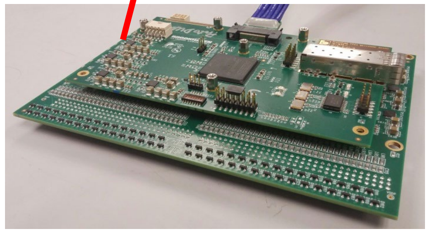


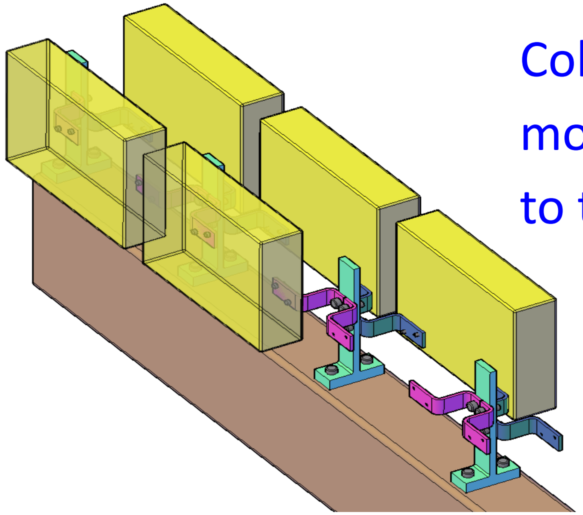


Integral design concept of APA + CE + Feed-through, plus Warm Interface Electronics with local diagnostics and strict isolation and grounding rules.

Strictly applied to ProtoDUNE resulted in low noise performance in a short time.



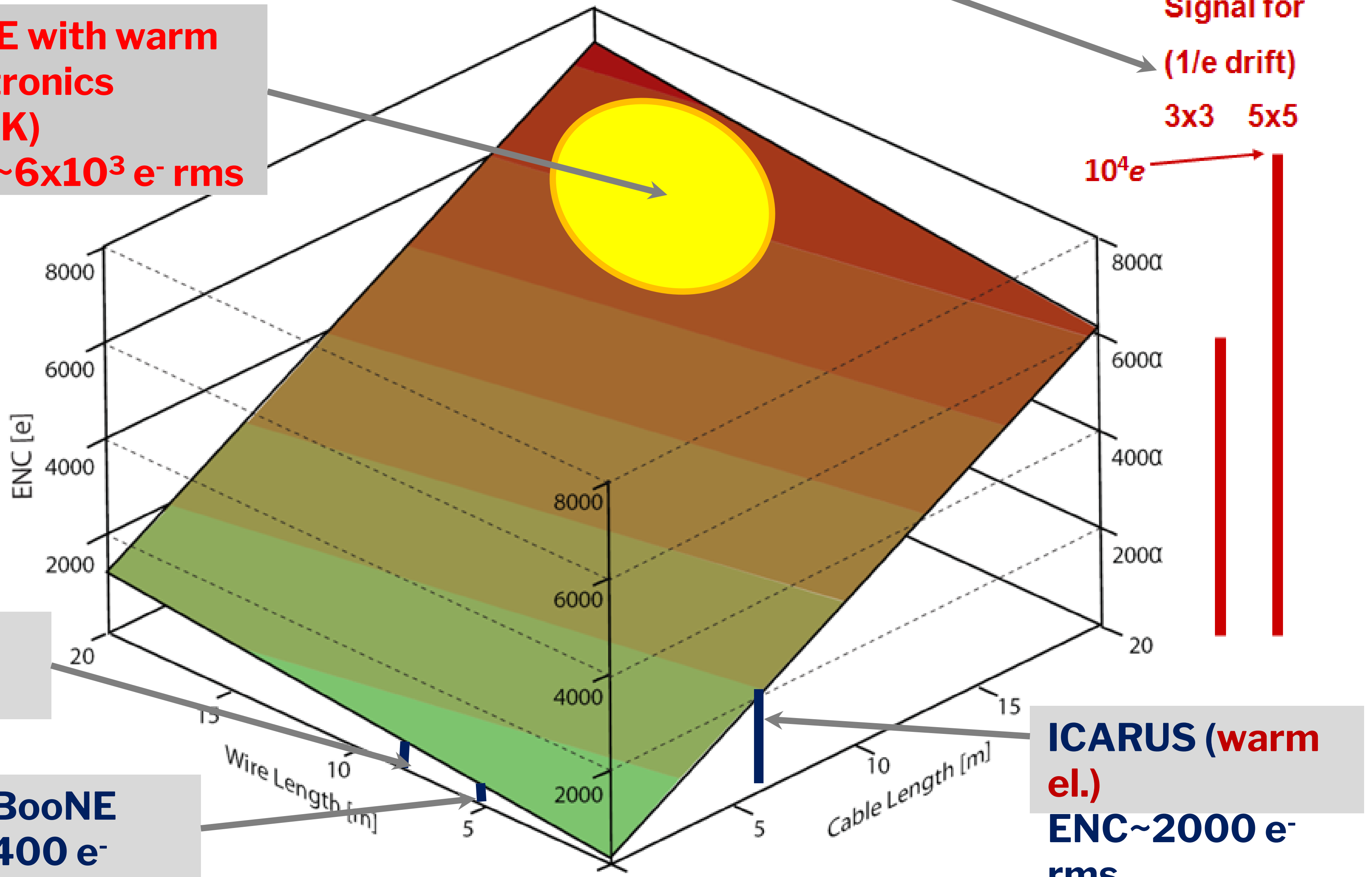




Cold electronics (CE) module and its attachment to the APA frame

Noise (ENC) *vs* TPC Sense Wire and Signal Cable Length for CMOS at 300K and 89K

MIP Signal for 3x3 and 5x5 mm Sense Wire Spacing



DUNE with warm electronics (300K) ENC~6×10^3 e^- rms

ProtoDUNE ENC~660 e^- rms

MicroBooNE ENC~400 e^- rms

ICARUS (warm el.) ENC~2000 e^- rms

Veljko. Radeka, Lidine 2021, Sept 14

Light sensing in noble liquid TPCs by Silicon Photo Multipliers (SiPMs) for **Large Area Photo Detectors**

Literature for in-depth study of SiPMs (mostly small devices, ≤3x3 mm^2, for PET and medical imaging)

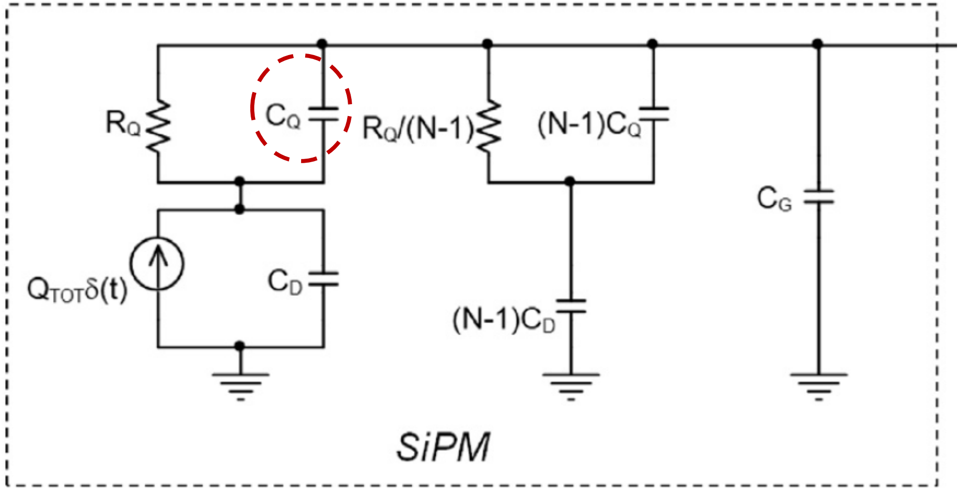
NIM A926 (2019), Special Issue on SiPMs

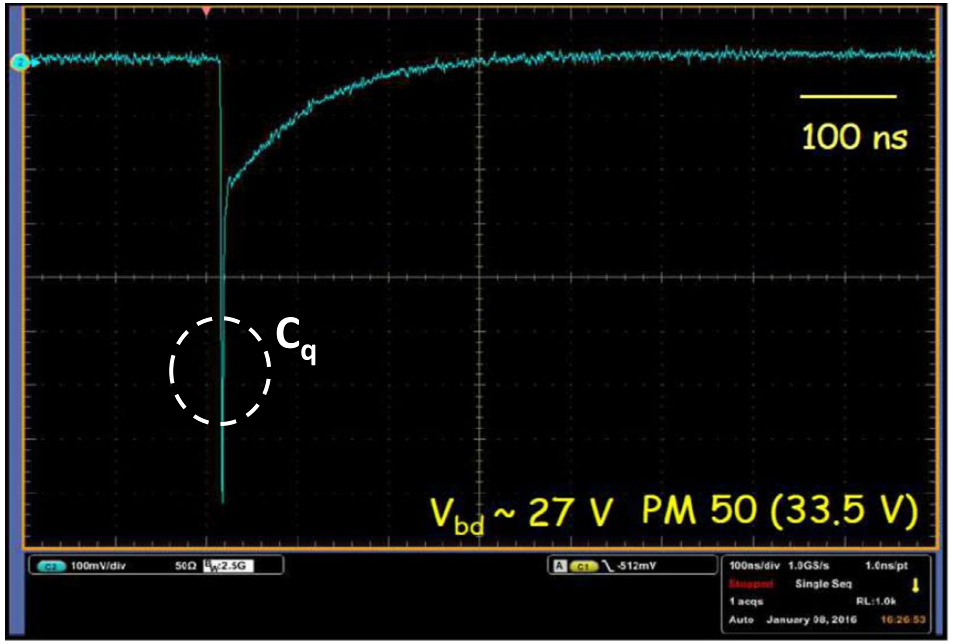
[1] R. Klanner, *Characterisation of SiPMs*

[2] F. Acerbi, S. Gundacker, *Understanding and simulating SiPMs*.

[3] P.P. Calo, F. Cicierello C. Marzocca, S. Petrognani, *SiPM Readout Electronics*.

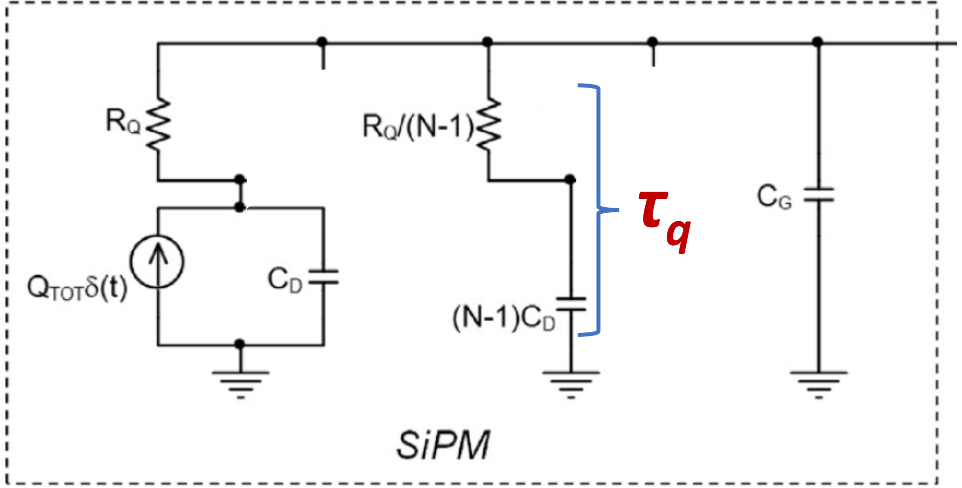
SiPMs for PET, ≤3x3 mm^2, Pixels ≈ 25 µm

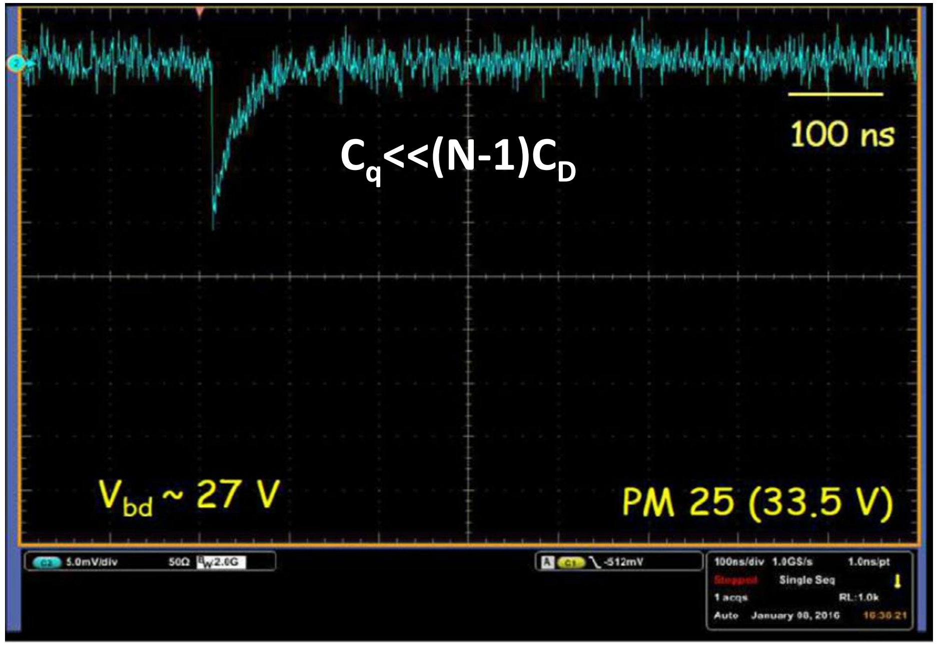




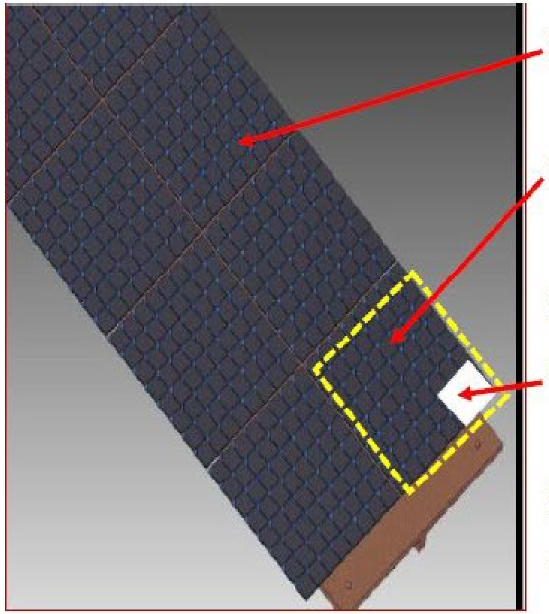
Adapted from: R. Klanner, NIM A926 (2019) 36

SiPMs for Noble Liquid TPCs, ≥6x6 mm^2, Pixels ≥ 50 µm





nEXO SiPM Light Detector Readout

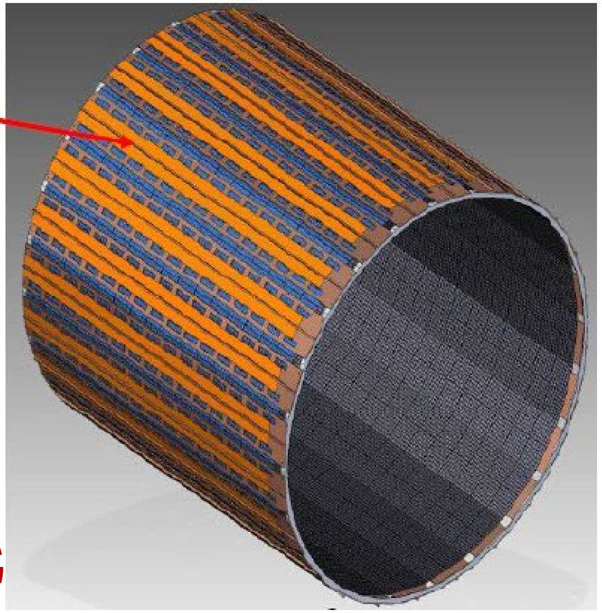


Staves: 24

Tiles : **24** x 2 x 10 = **480**

Sub-arrays 6 cm^2:
480 x 16 = **7680**

SiPM Area: **7680** x 6 cm^2=
= **4.6 m^2**

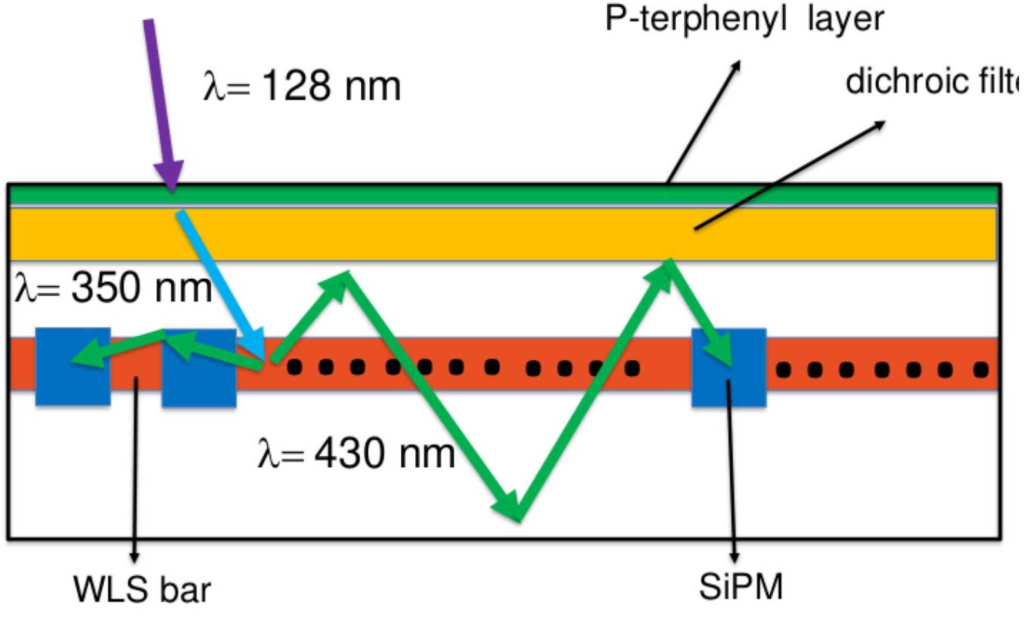


Technology	"HPK"	"FBK"
C/A [nF/cm^2]	3.5	8.5
V_{op} [V]	50	30
C_{6cm^2} [nF]	**21**	**51**
C_{2s} [nF]	**5**	**12.5**
V_{2s} [V]	100	60

Readout challenge:
Fine segmentation, 7680 SiPM subarrays=electronic channels (<1 p.e/subarray), still results in a "giant" subarray capacitance/channel, ~**5-12 nF** in the best case (series connection C_{2s}), and ~**20-50 nF** in the worst case (SiPMs in parallel).

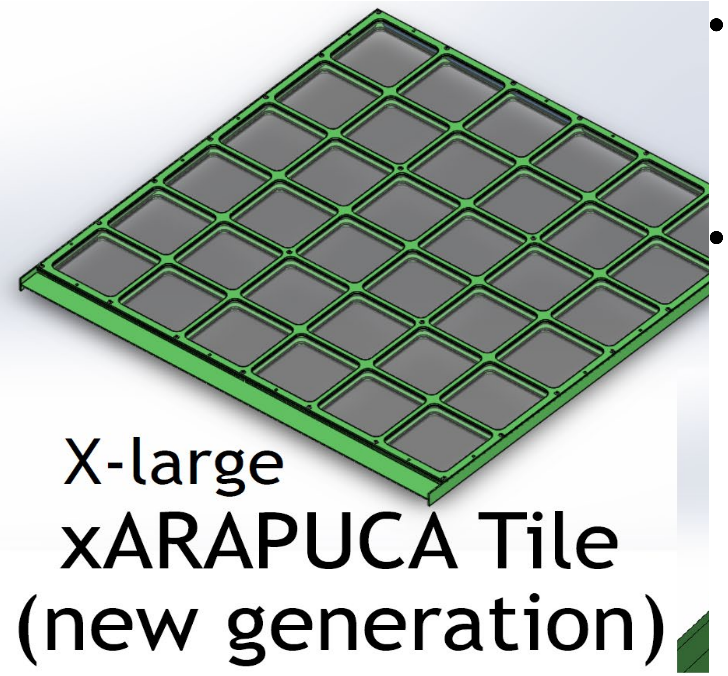
SNR>10 for single photo electrons essential for nEXO!

DUNE FD-2: ARAPUCA (Argon R&D Advanced Program at UniCAmp).



Credits: F. Terranova

- ➢ 160 SiPMs (40 per side)
  - ➢ Glued to WLS Bar for improved optical contact
- ➢ SiPMs mounted on Kapton flexi-PCB



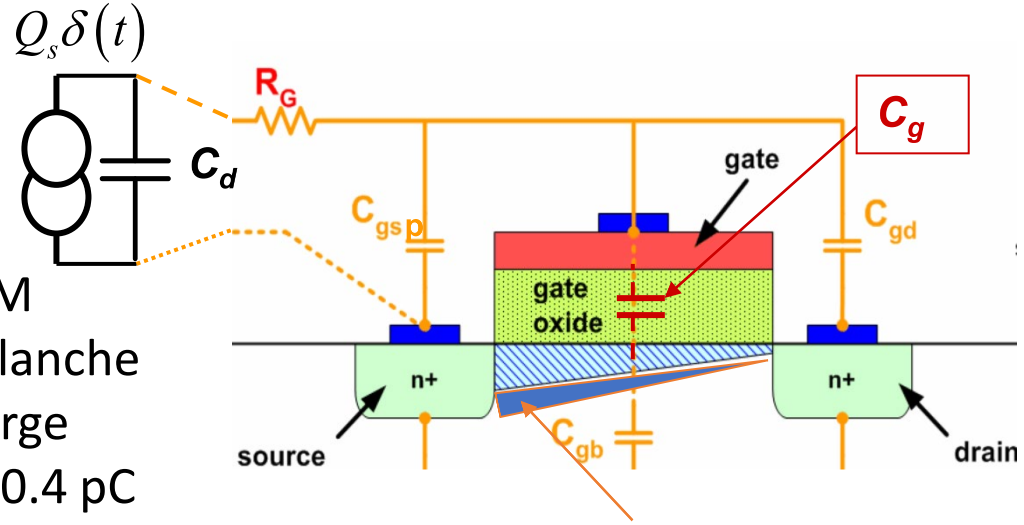
X-large xARAPUCA Tile (new generation)

- **Optical area**
  - **600 mm x 600 mm=3600 cm^2**
- **SiPM area**
  - **160 x 0.36 cm^2 ≈60 cm^2**
  - **≈1.7 % of opt. area**
  - **SiPM array capacitance ≈200 nF for V_{bd}~45 V;**
  - **≈260 nF for V_{bd}~37 V**

Readout a challenge for DUNE and SBND!

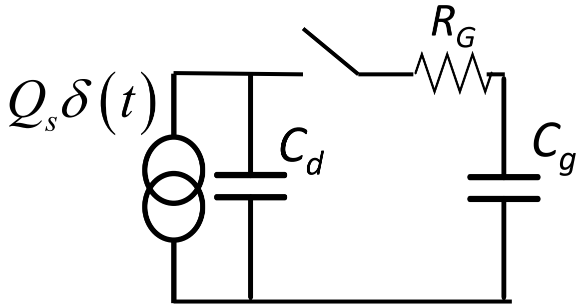
M.C. Queiroga Bazetto, V.L. Pimentel, A.A. Machado and E. Segreto, in Campinas, Brazil

How much of the avalanche charge can we really "see"?
SiPM – transistor capacitance mismatch



SiPM
avalanche
charge
$Q_s \approx 0.4$ pC

"useful" charge: Q_g modulates the channel and with transistor noise determines S/N



$$\frac{Q_g}{Q_s} = \frac{C_g}{C_g + C_d}$$

Example:

Transistor gate: C_g **=25pF** (very large transistor)

	nEXO	xARAPUCA
SiPM array: C_d	**≥20 nF**	**>200 nF**
$(Q_g/Q_s)=(Cg/Cd)$	**≤1/800**	**≤1/8000**

We "see" ~ **1 part in 10^3 or 10^4** of the SiPM avalanche charge Q_s.

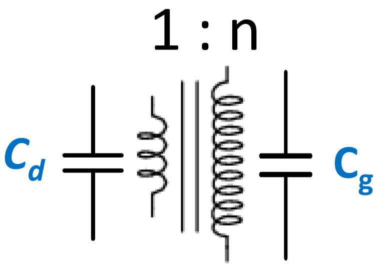
A long way from the optimal sharing of charge:

$(Q_g/Q_s)_{max}$ **= 1/2**
for $(Cg/Cd)=1$

SiPM-to-transistor capacitance matching: *SNR* vs transformation ratio *n*

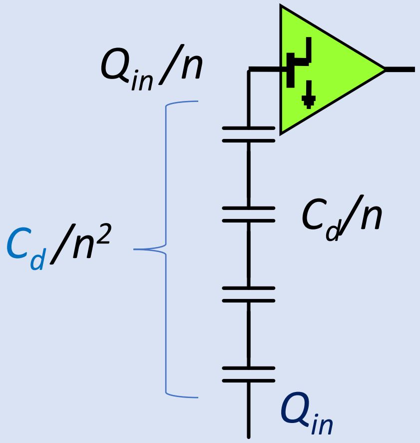
$$n_{opt} = \left(\frac{C_d}{C_{gs}}\right)^{1/2} \qquad \left(\frac{S}{N}\right)_{(n)/(n=1)} \simeq n_{opt}\frac{n/n_{opt}}{1+\left(n/n_{opt}\right)^2} \qquad \left(\frac{S}{N}\right)_{(\max)/(n=1)} = \frac{n_{opt}}{2}$$

n= transformation ratio for ***EM and ES transformers***; for ***transistors in parallel***: $n = n_{trans}^{1/2}.$



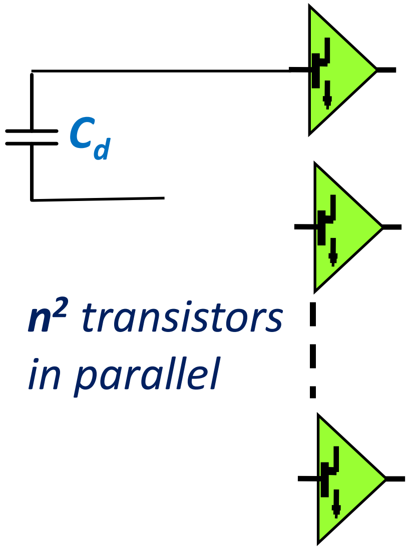
EM transformer, most effective and proven, but not radio pure (introduced 1974)

For C_d=20 nF, C_g=25 pF → *n_{opt}={C_d/C_g)^1/2~***28, *S/N*** is **increased by *n_{opt}*/2=14**



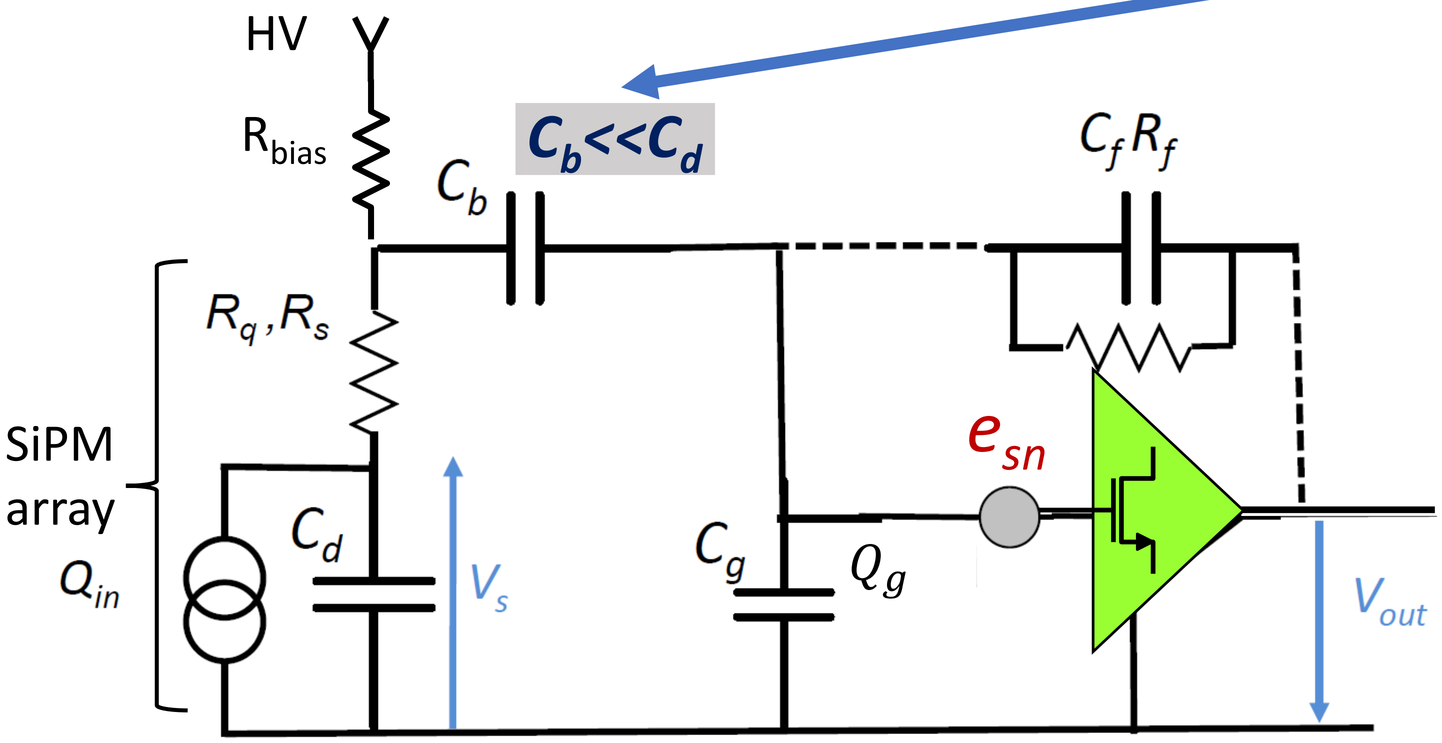
ES (Electrostatic) transformer
(introduced 1990)

ES transformer n=4 improves *S/N* by a factor of ~ 3.95 ;
compared to parallel connection of SiPMs.



For n=4, it would take ***n^2*=16,** times as large a transistor area ***and power*** for the same result as with EM or ES transformer.

Optimal readout for SiPM arrays: Weak coupling to amplifier



Basic limitation: Only ***adiabatically*** *transferred fraction of avalanche charge to transistor gate,* $Q_g \approx \frac{C_g}{C_d} Q_{in}$ *contributes to S/N.*

Conventional approach: Strong coupling -- *active (forced) transfer of charge* is accompanied by corresponding increase in noise ***with no benefit to S/N***. It requires **$C_b \gg C_d$**, resulting in (de)coupling capacitors in ***tens of nanofarads.***

Q_{in}= avalanche charge
*C_d=*capacitance of SiPM array in parallel;
***n* = ES transformation ratio**

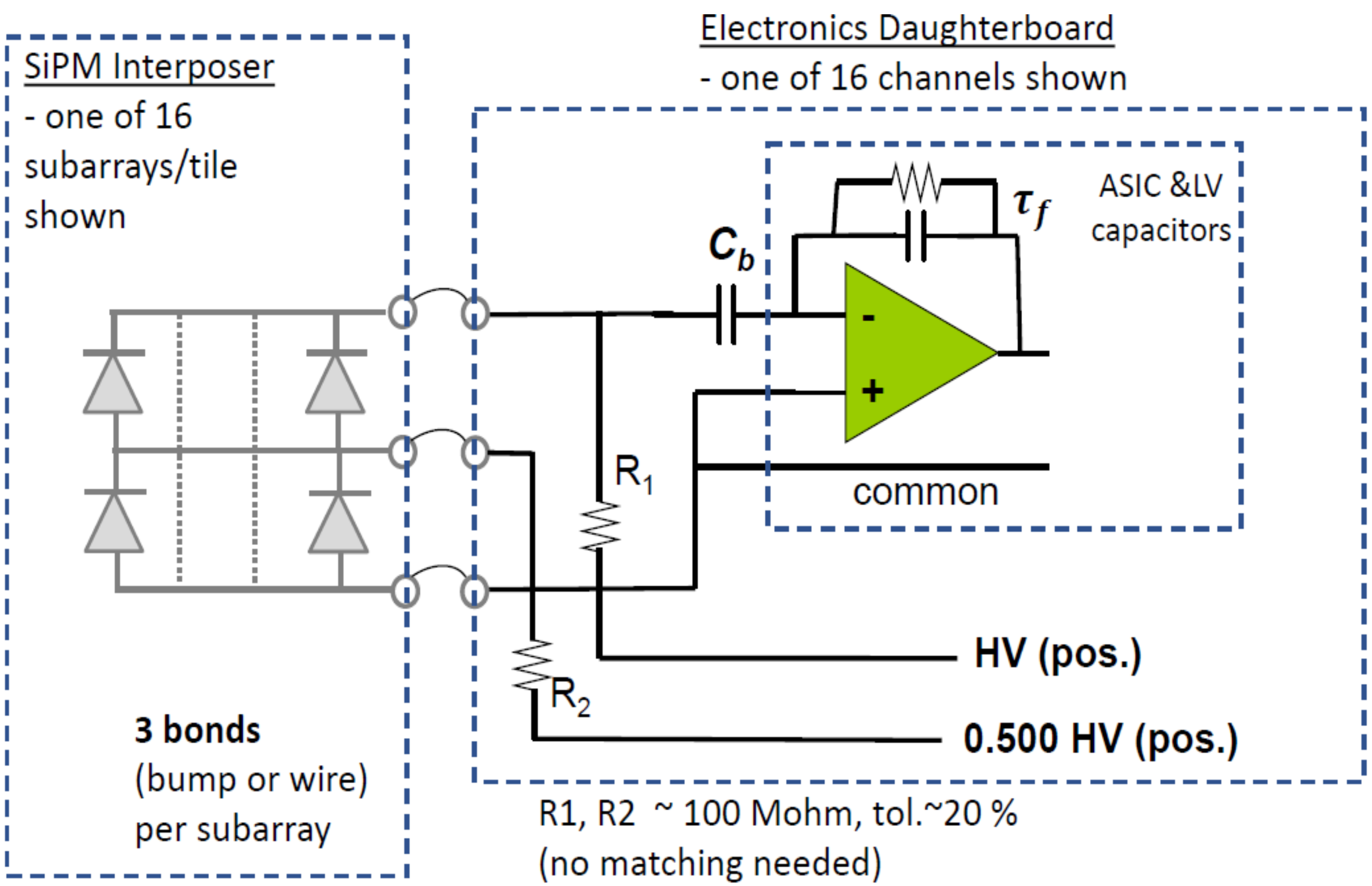
$$\left(\frac{S}{N}\right)_n = \frac{Q_{in}/C_d}{e_{sn}/t_p^{1/2}} \cdot \frac{n}{1 + C_g/C_b + n^2 C_g/C_d}$$

S/N analysis *shows:* ***C_b*** *must be larger than* ***C_g****, but can be* ***much smaller*** *than* ***C_d****:*

$C_d \gg C_b \gg C_g$

e.g., 20 nF>>0.5 nF>>25 pF

BNL: Demonstration of 6 cm^2 SiPM(HPK) 20 nF subarrays with LAr ASIC in LN2



R1, R2 ~ 100 Mohm, tol.~20 %
(no matching needed)

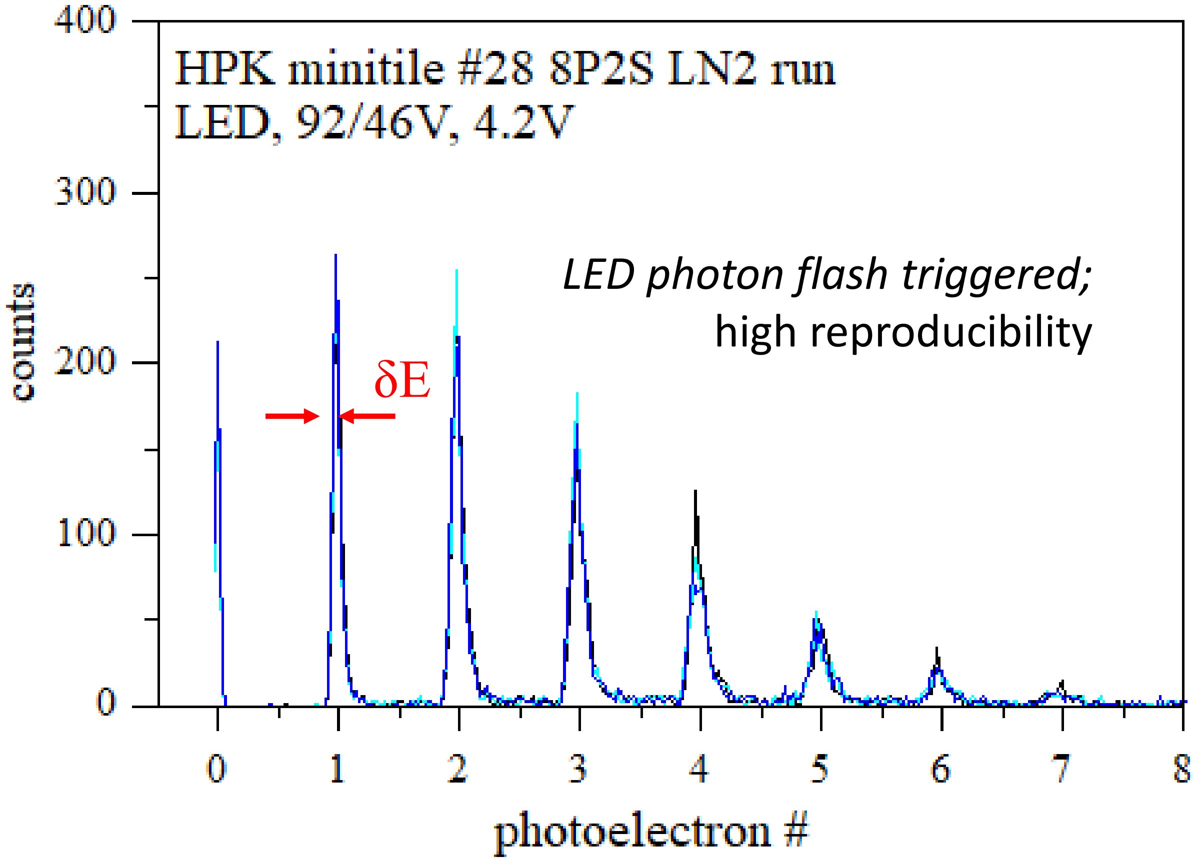
Electrostatic Transformer (series connection of SiPMs) ***n*=2** shown; readout scheme is independent of ***n***

“Weak coupling” (Cb<<Cd) vs conventional strong coupling (Cb>>Cd):

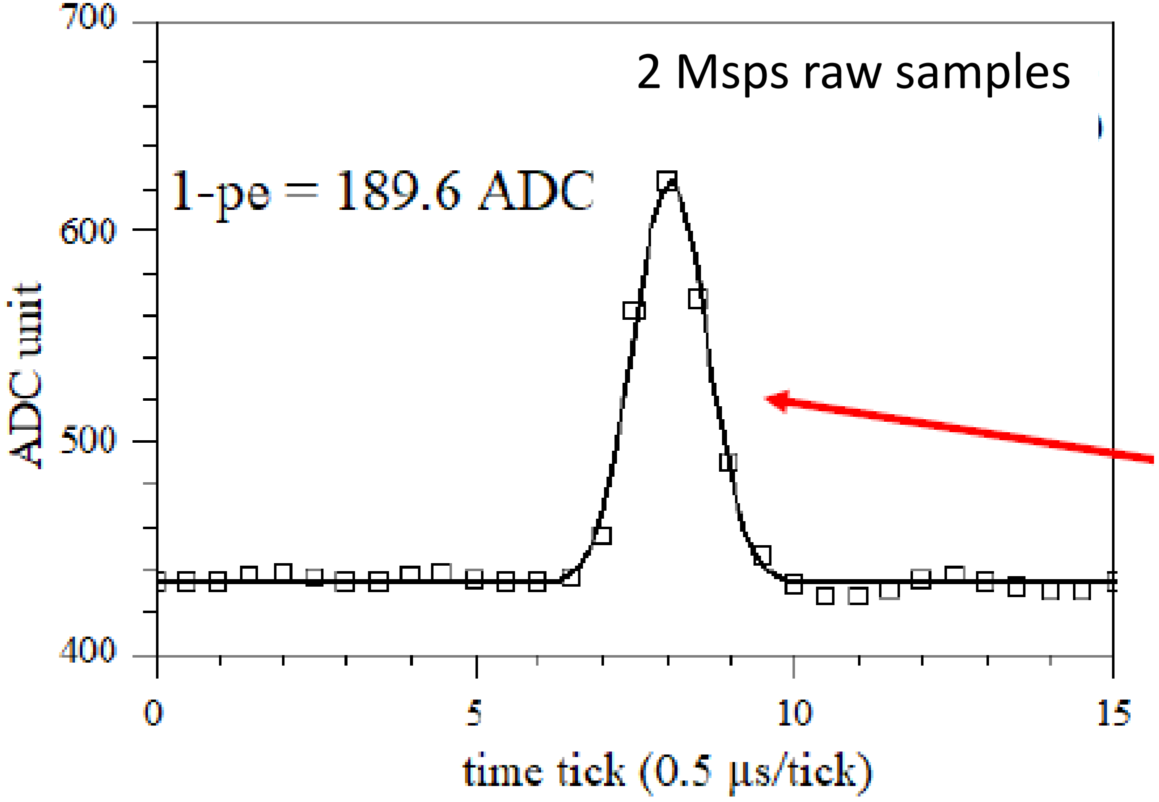
- **Radiopure 500 pF/100 V capacitor** easier to realize, and lower risk than 50 nF/100V;
- **Calibration and diagnostics** of electronics independent of SiPM capacitance and condition (open or short).
- **Small C_b allows higher inductance interconnections.**
- In situ SiPM array capacitance measurement.

Concept, realization, tests by
H. Chen, S. Gao, V. Radeka, S. Rescia, T. Tsang

BNL: Demonstration of 6 cm^2 SiPM(HPK) *__20 nF subarrays__* with LArASIC in LN2



LED photon flash triggered;
high reproducibility



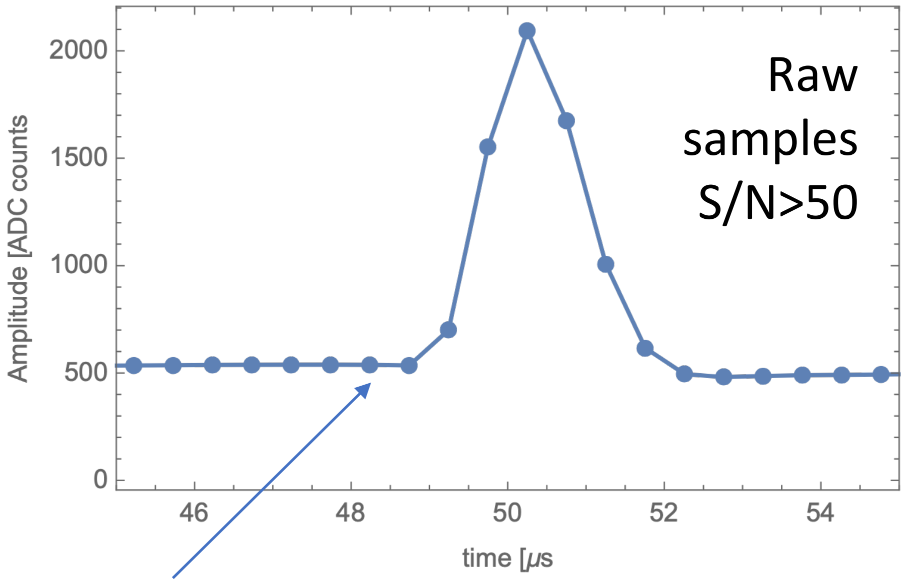
Photon rate: ~80 Hz (trigger rate 100 Hz)

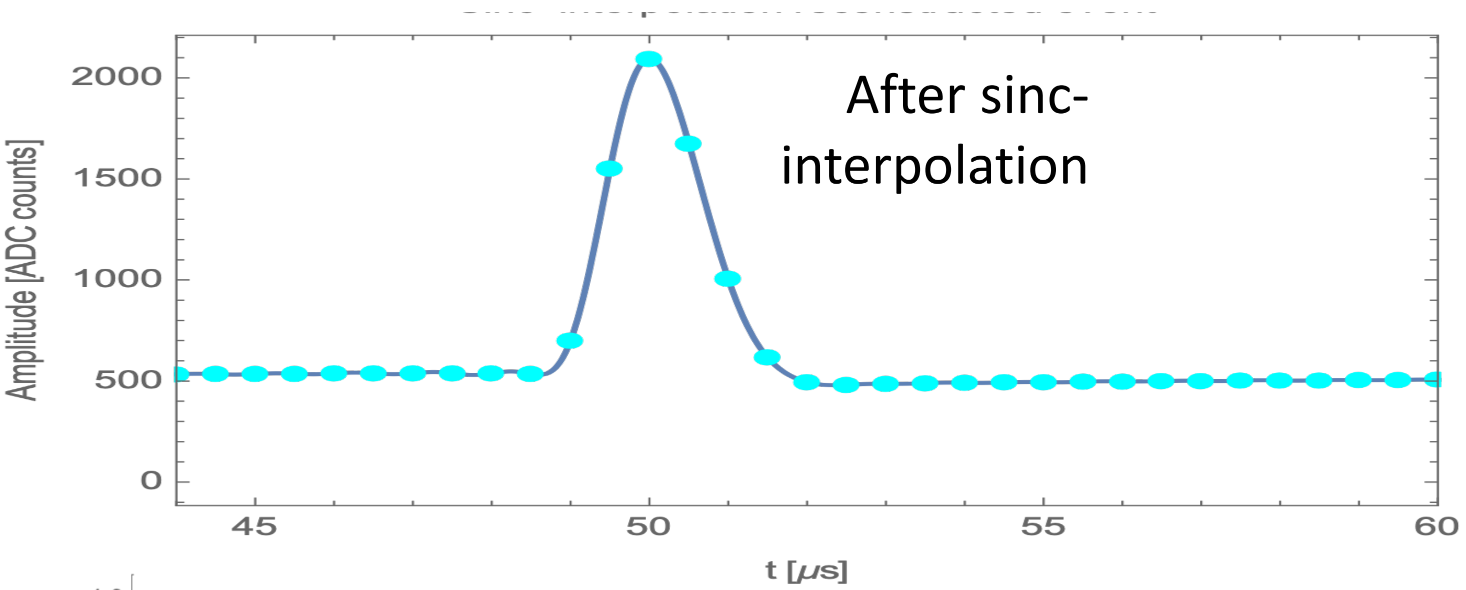
Single photoelectron waveform information provided by a "snippet" of samples :

1-pe resolution (δE): 3 to 3.5% rms

- **1-pe *S/N* ~60 ; avalanche = 0.4 pC at OV=4 V**
- **1-pe *coincidence resolution* __between two subarrays__ < 20 ns**

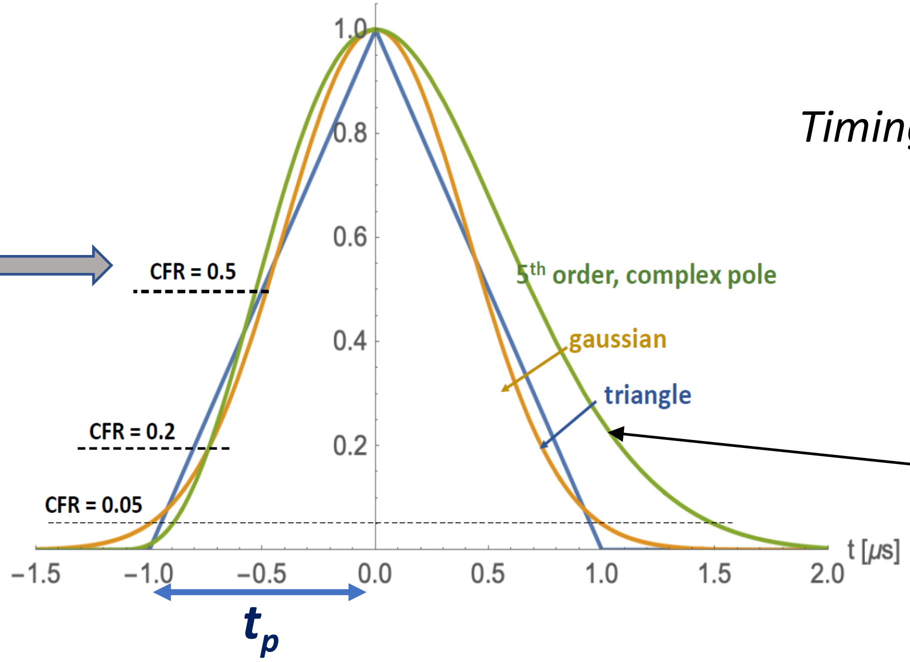
Waveform reconstruction and 1-pe timing resolution (SPTR)





Waveform snippet:
10 μs = 20 samples at **2Msps**;
***t*$_p$=1μs** anti-aliasing filter (as per **Nyquist**: ***t*$_p$≥2/*f*$_s$**)

Using ***sinc-interpolation*** +
'digital' constant fraction
discriminator, results in a
low timing error (SPTR)



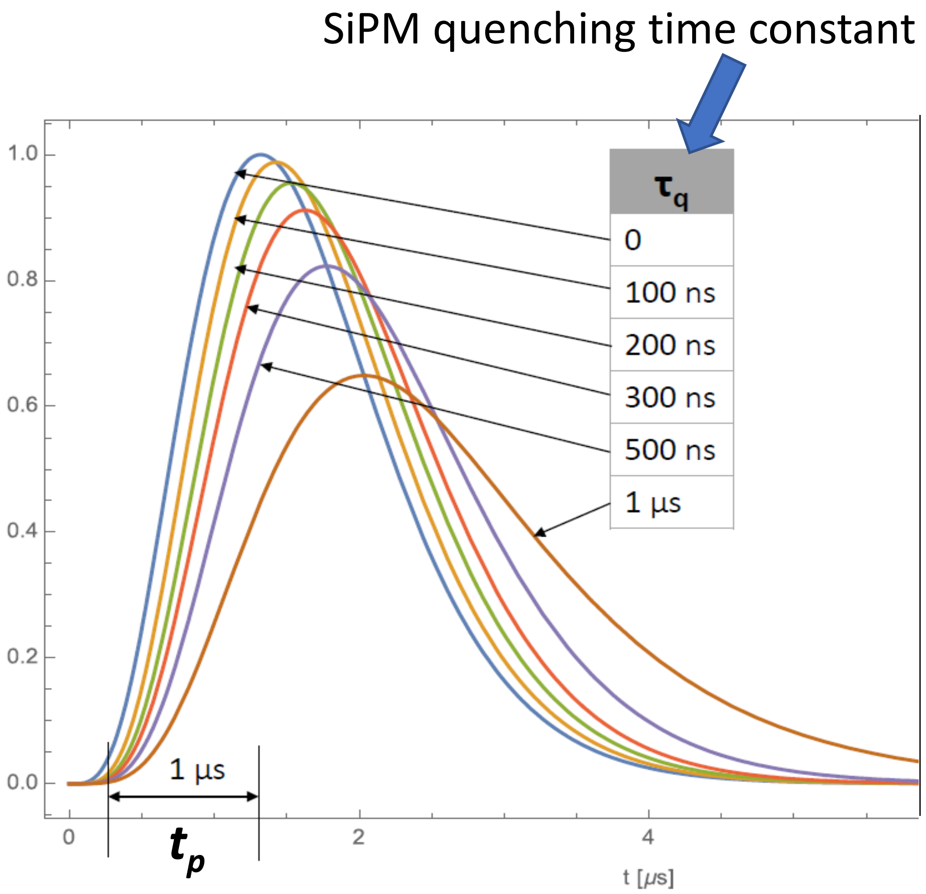
Timing resolution:

$$\sigma_t = \alpha_f \frac{t_p}{(S/N)}$$

$$\alpha_f = shape\,const. \approx 0.63$$

(for 5th order complex pole)

Is SiPM design optimal for large Area Photo detectors?: The role of Quenching Time Constant τ_q (and quenching resistance)



Long quenching time constant and short integration time makes the signal increasingly difficult to detect.

S/N with ES transformation by ***n***:

$$\left(\frac{S}{N}\right)_n = \frac{Q_{in}/C_d}{e_{sn}/t_p^{1/2}} \cdot \frac{n}{1+C_g/C_b+n^2 C_g/C_d}$$

Q_{in}= avalanche charge
C_d= capacitance of *all SiPMs in the array connected in parallel*
C_g/C_d ≈0.05 for weak coupling (slide 18)
t_p= peaking ("integration") time of anti-aliasing filter
e_{sn}=noise spectral density of input transistor

xARAPUCA: single channel 1pe *S/N*=12.5 at ***n*=4, t_p=1us, t_q=100ns**

t_p	t_p =100ns	t_p =500ns	t_p =1μs
τ_q=100ns	Ball def=0.58 1pe S/N=2.9 SPTR=31ns	ball def=0.93 1pe S/N=9.4 SPTR=37ns	ball def=0.98 1pe S/N=12.5 SPTR=53ns

t_p	t_p =100ns	t_p =500ns	t_p =1μs
τ_q=500ns	ball def=0.2 1pe S/N=1 SPTR=110ns	ball def=0.58 1pe S/N=5.9 SPTR=76ns	ball def=0.77 1pe S/N=9.8 SPTR=81ns

Summary

- With a large SiPM array capacitance grossly mismatched to even the largest input transistor, active (forced) transfer of charge from SiPM via a large (de)coupling capacitor (**$C_b>C_d$,**i.e., strong coupling) does not benefit ***SNR***. In such a forced (*non-adiabatic*) transfer of charge by a “current amplifier/conveyer”, “transimpedance”, or any similar, ***SNR*** is limited by the noise of the amplifier (in the limit by the input transistor).
- In case of such a large capacitance mismatch, **a *weak coupling* between the SiPM and input transistor is sufficient**, where **$C_d>>C_b>>C_g$**. A charge sensitive amplifier (CSA), or a “voltage amplifier” is coupled to a SiPM parallel/series array by a decoupling capacitor only an order of magnitude larger than transistor capacitance, and independent of a much larger SiPM array capacitance **(C_b~200-500pF for a SiPM array of 10 nF, or even 100 nF).**
- **SiPMs with lowest capacitance (higher V_{bd}), offer better *SNR* and timing resolution in large area photo detectors. SiPMs with the lowest quenching time constant at low temperature (allowed by the quenching process, e.g., ~100 ns) offer the best SNR, especially at shorter integration times.**
- **SiPMs with higher capacitance and long quenching time result in higher overall detector system cost (complexity, power, cabling) to achieve equal *SNR* and timing resolution.**

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- Insight into SiPM design:
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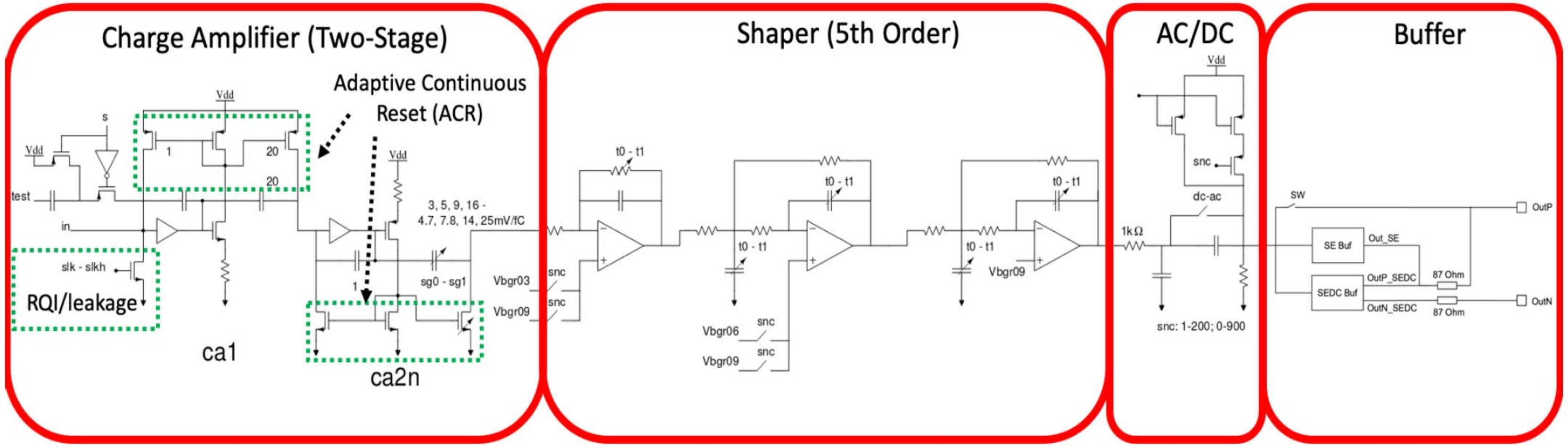
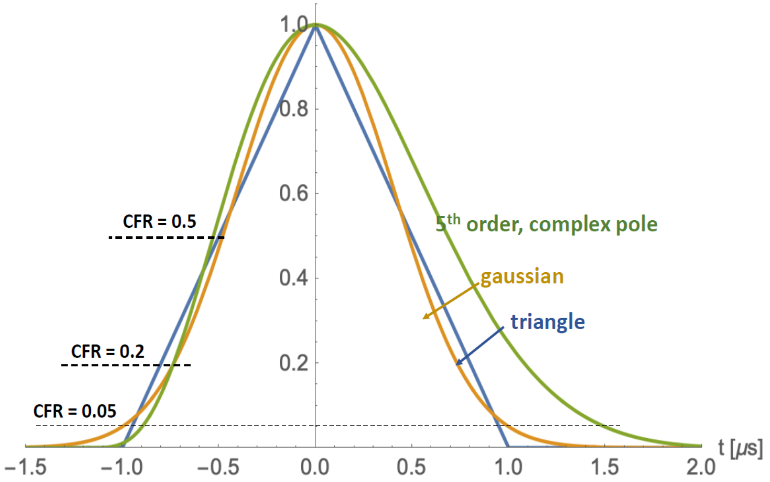
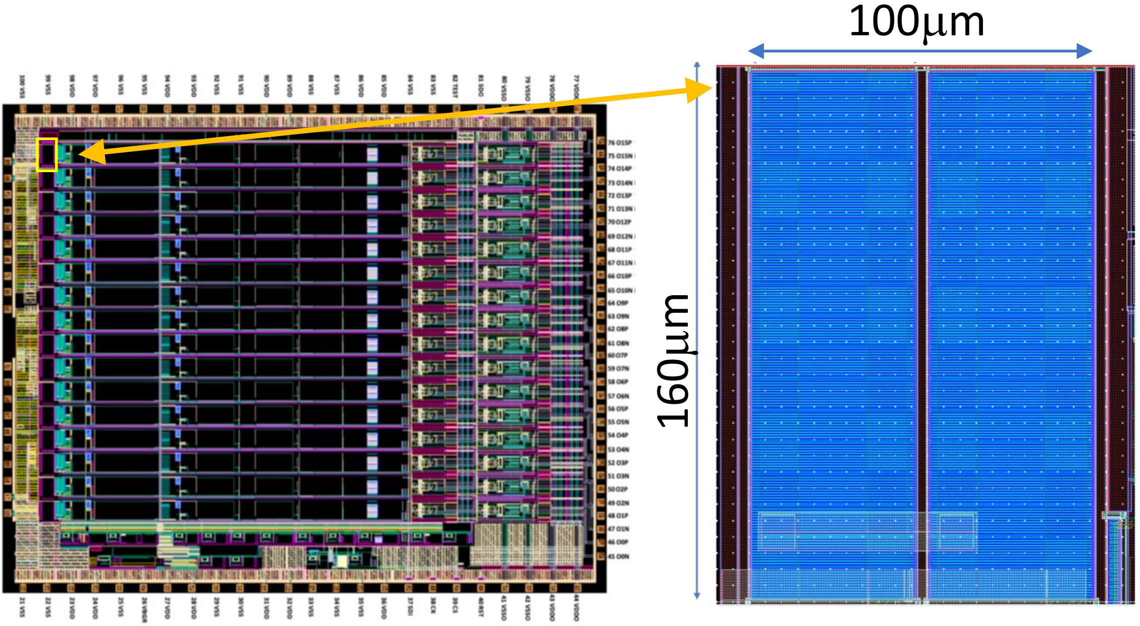
Appendix

LArASIC = Antialiasing Filter

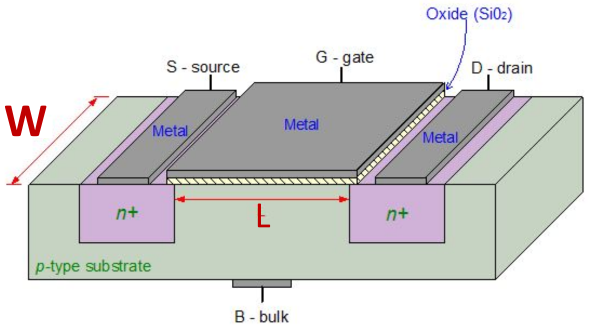






160µm x 100µm=16,000µm^2

$$W/L = \frac{20\ mm}{270\ nm}$$



For a *very large low noise PMOS transistor:* W/L~4x10^4, C_g~20pF ; *This very large transistor is a small fraction of the SiPM array capacitance (20-200 nF!)*

Why not an even larger transistor?

The equivalent noise resistance is smaller than SiPM quenching resistance and interconnections resistance (<10 ohms).