

Assembly and characterization of a large area VUV sensitive SiPM array for the nEXO TPC test stand at Stanford

Jacopo Dalmasson
LIDINE conference
14 September 2021

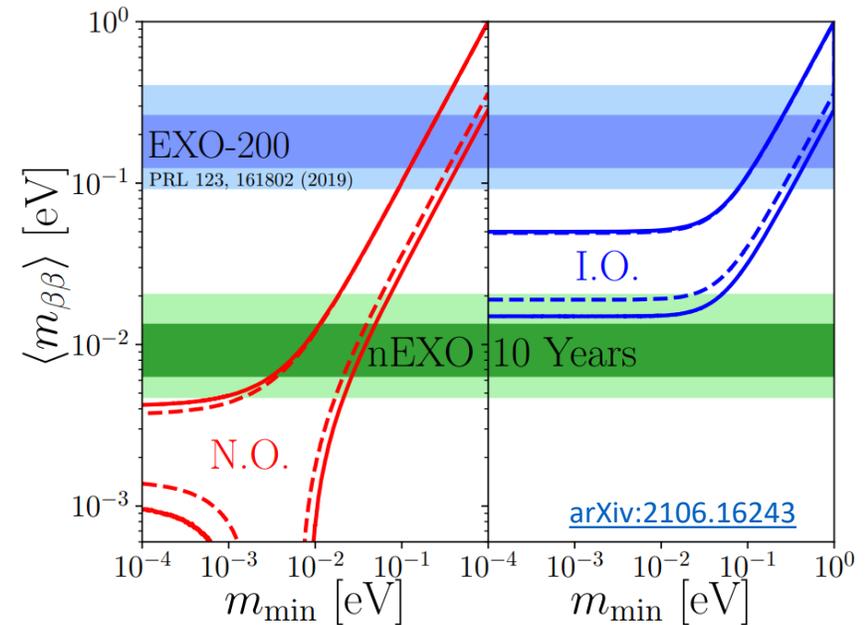
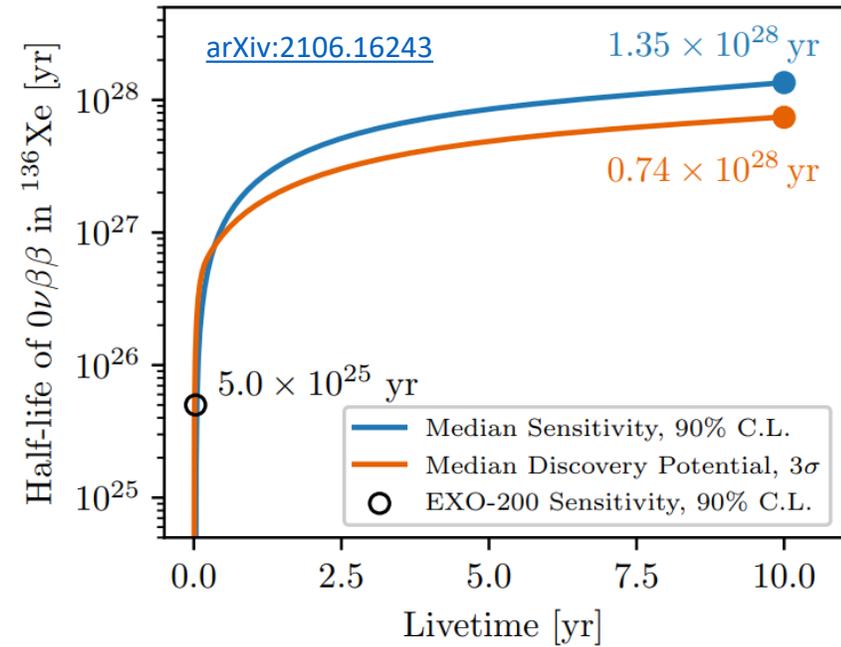
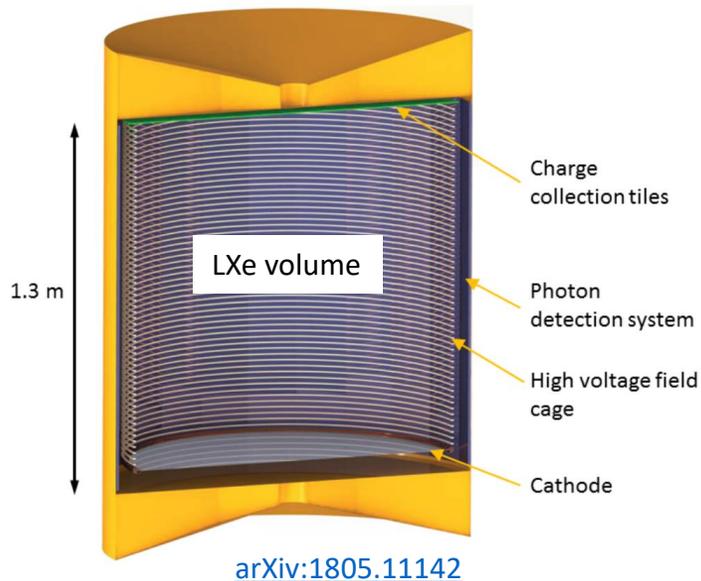


Outline

- The nEXO Experiment
- Motivation
- Current Setup
- Large Area SiPM Array Upgrade
 - Assembly
 - SiPMs
 - Front End Readout
- Preliminary Tests
- Light Simulation
- Next Steps and Conclusion

The nEXO Experiment

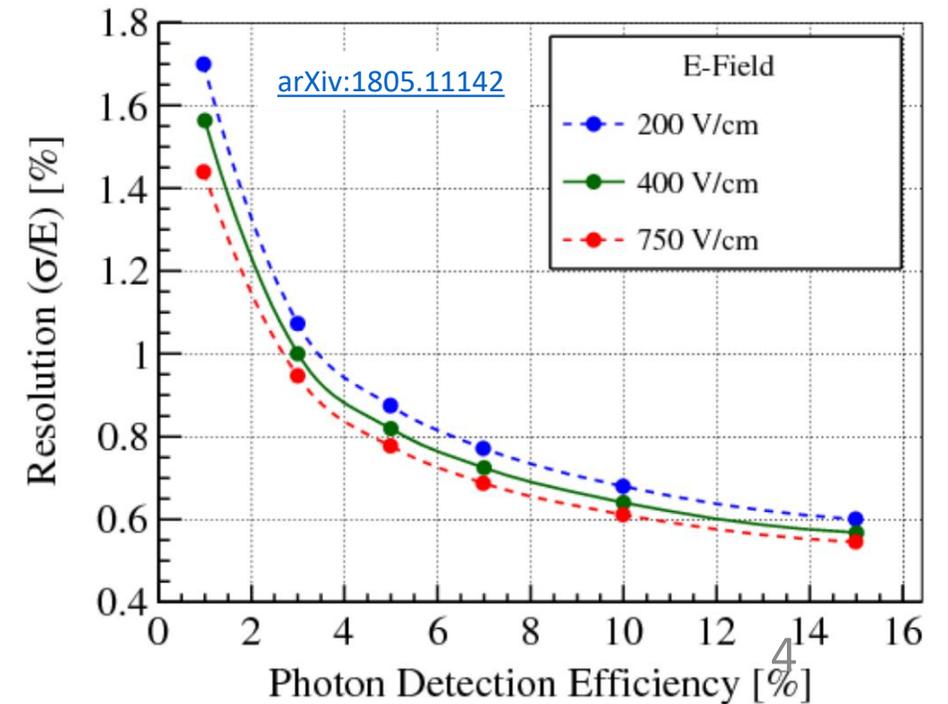
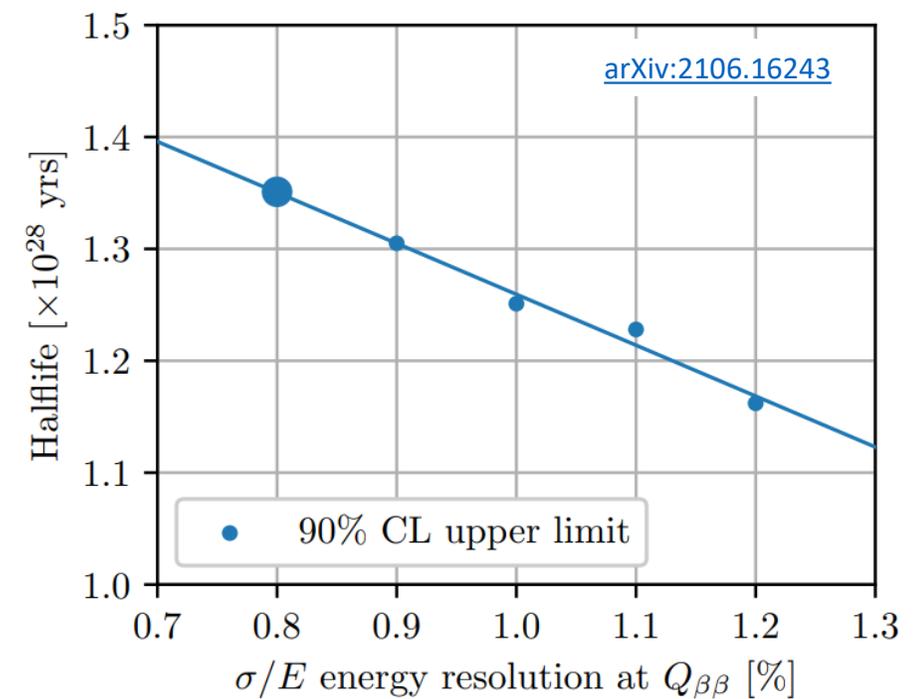
- 5 tonnes $\sim 90\%$ enriched ^{136}Xe TPC aiming to fully explore the neutrino Majorana mass in the inverted ordering
- Projected sensitivity to neutrinoless double beta decay after 10 years exposure (90% CL) $\sim 10^{28}\text{y}$



Motivation

Three main observables are crucial to reach such result:

- Energy resolution
- Topology
- Event location



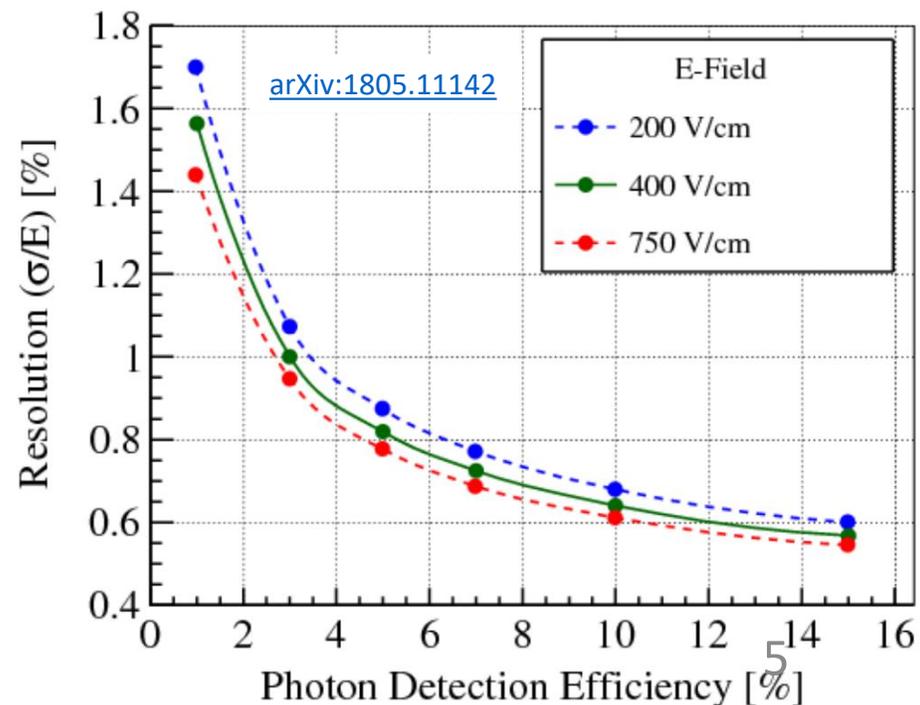
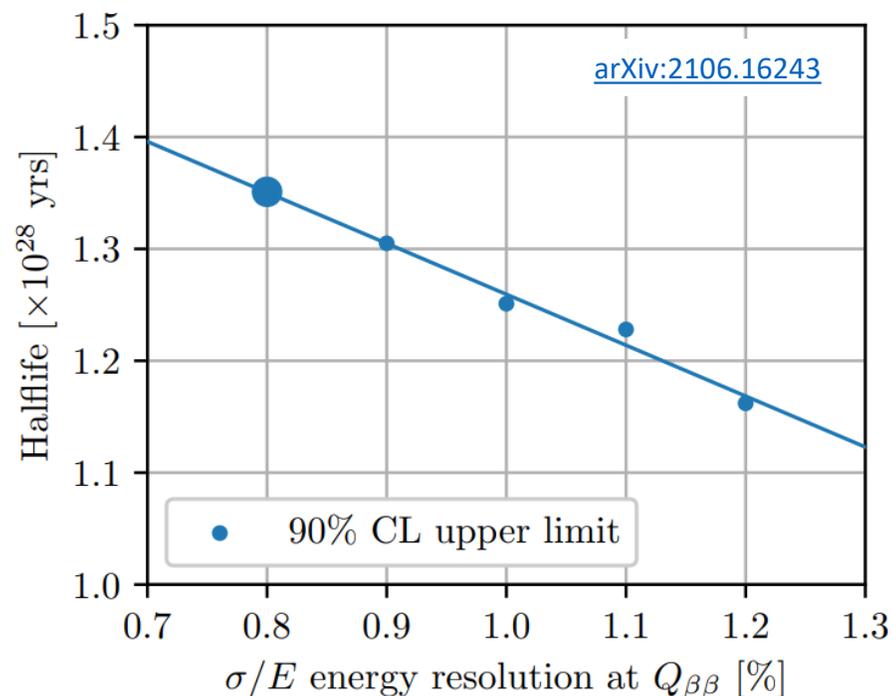
Motivation

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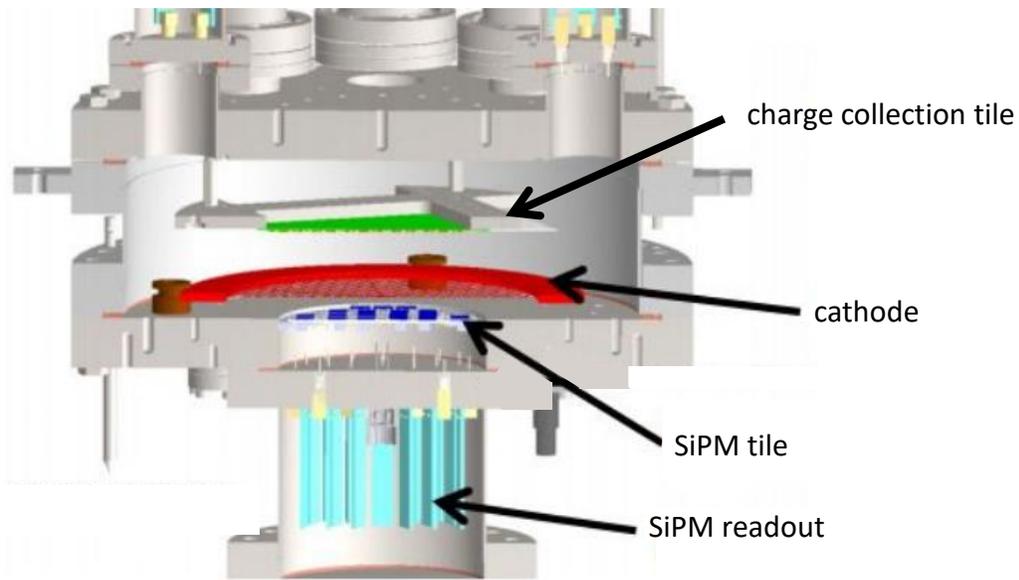
- Energy resolution
- Topology
- Event location

The resolution depends, among other parameters, on light collection efficiency.

In this work I'll describe the Stanford setup built to study this dependence



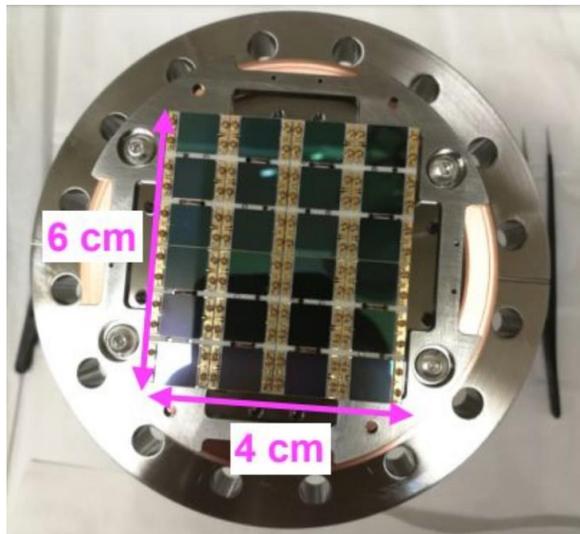
Current Setup



Mainly developed to characterize the charge tile [[arXiv:1710.05109](https://arxiv.org/abs/1710.05109)]. The light is mainly used from triggering and drift time calculation.

Light readout features:

- 24 $1 \times 1 \text{cm}^2$ SiPMs ganged into 12 channels
- Cold frontend electronics



Large Area SiPM Array Upgrade

10 fold increase in light-sensitive area:

- SiPMs epoxied and wirebonded on two ceramic tiles
- 32 channels (gang of 6 SiPMs/ch)
- Signal carried out from the cell via Kapton flex boards

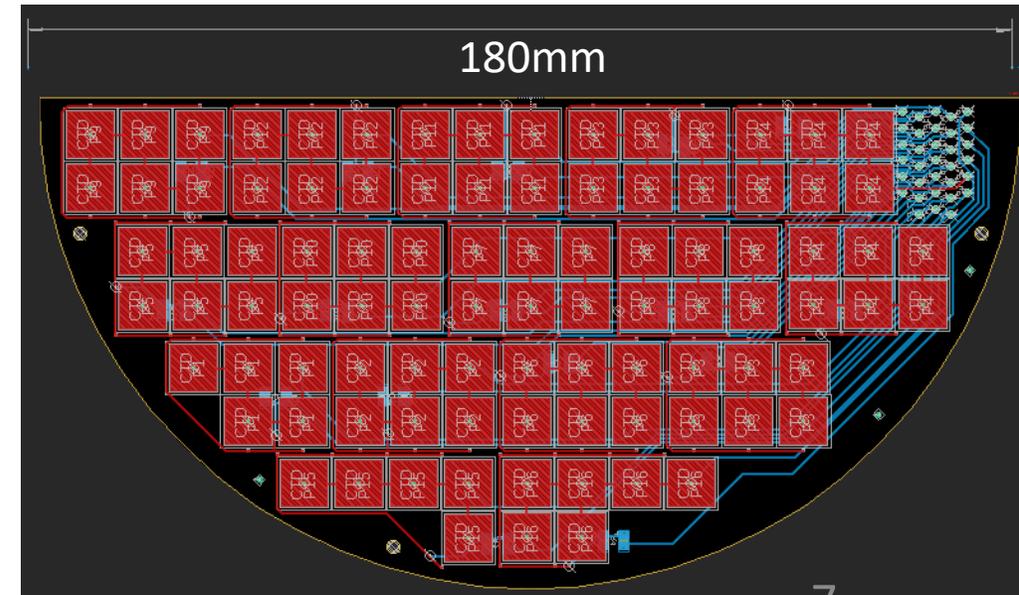
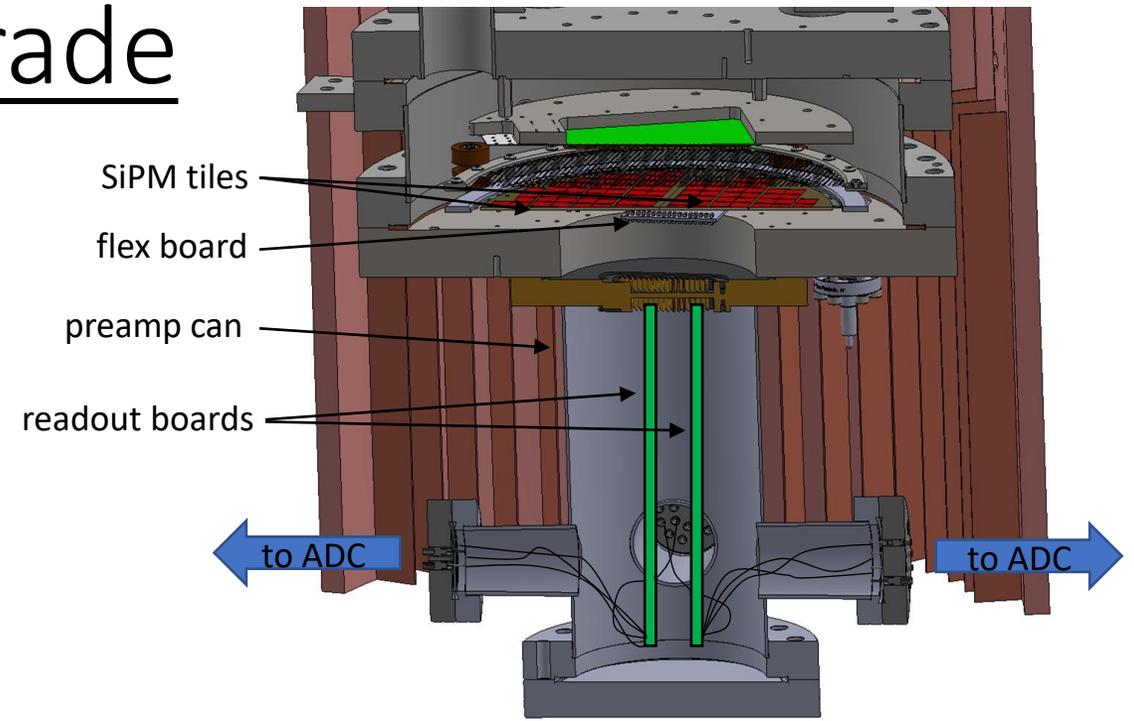
LXe

Signal is amplified with 2 readout boards (16 channels each)

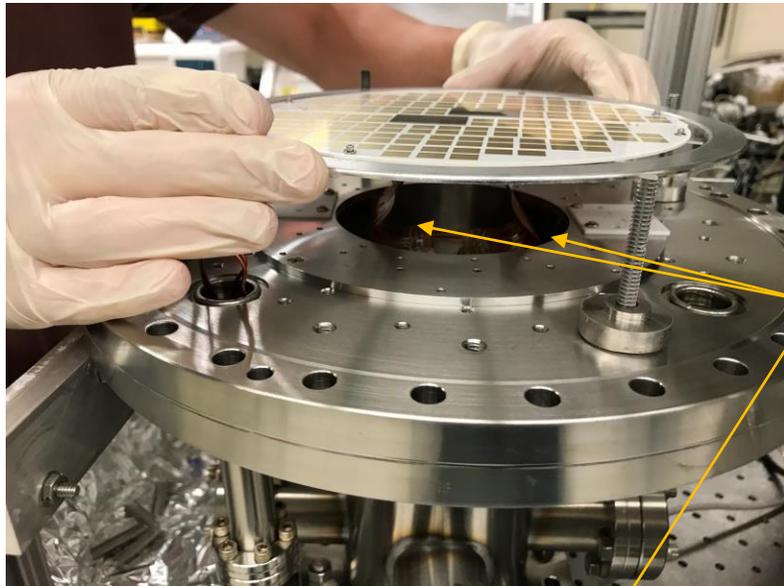
Cold

Finally digitized with a 16bit ADC

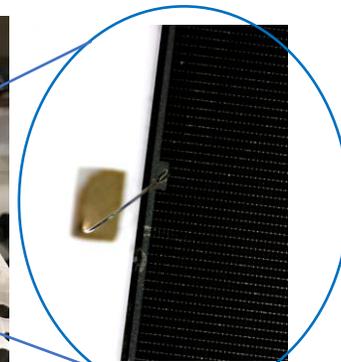
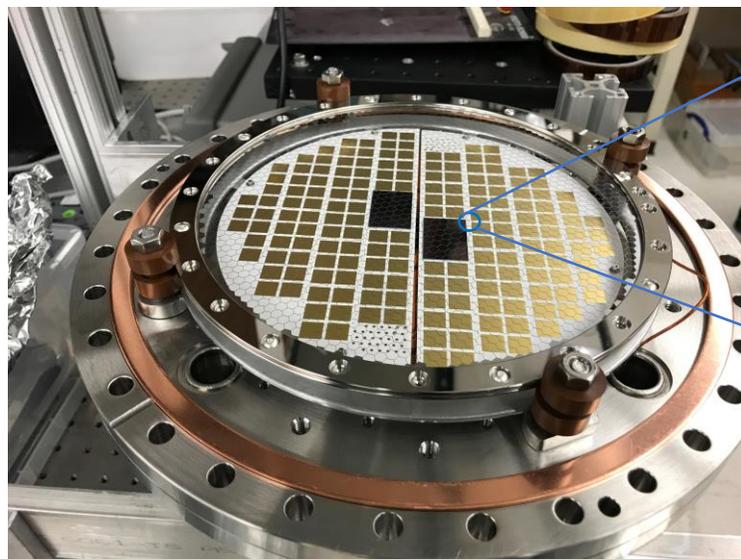
Room



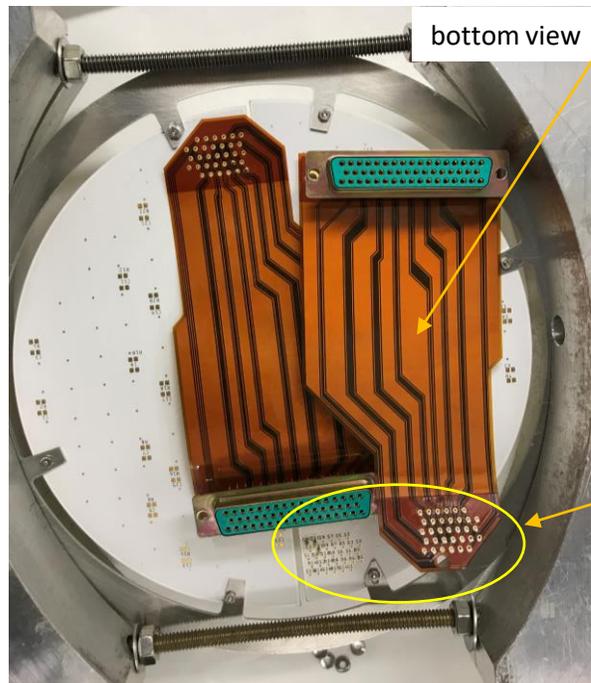
Assembly



flex boards

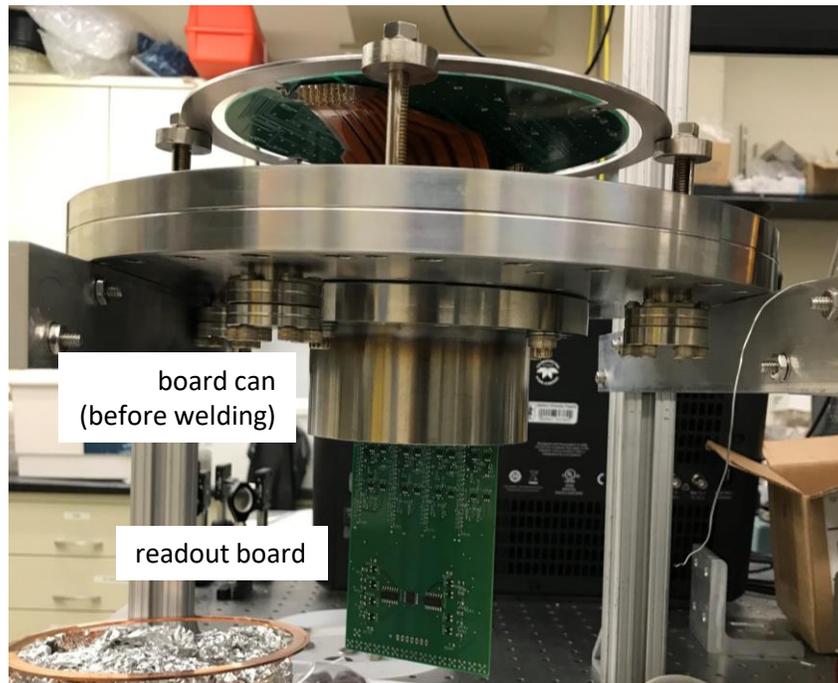


wire bond detail



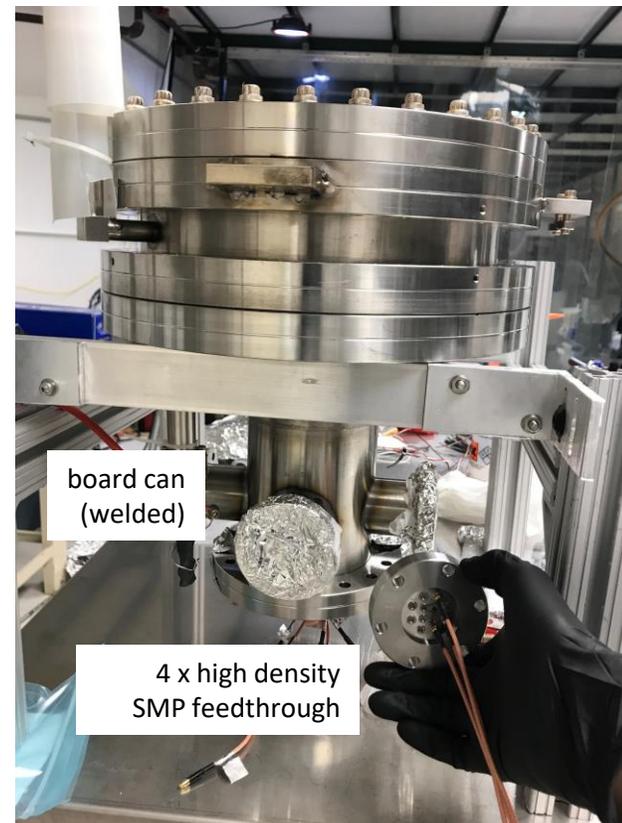
bottom view

pin/receptacle connection



board can (before welding)

readout board

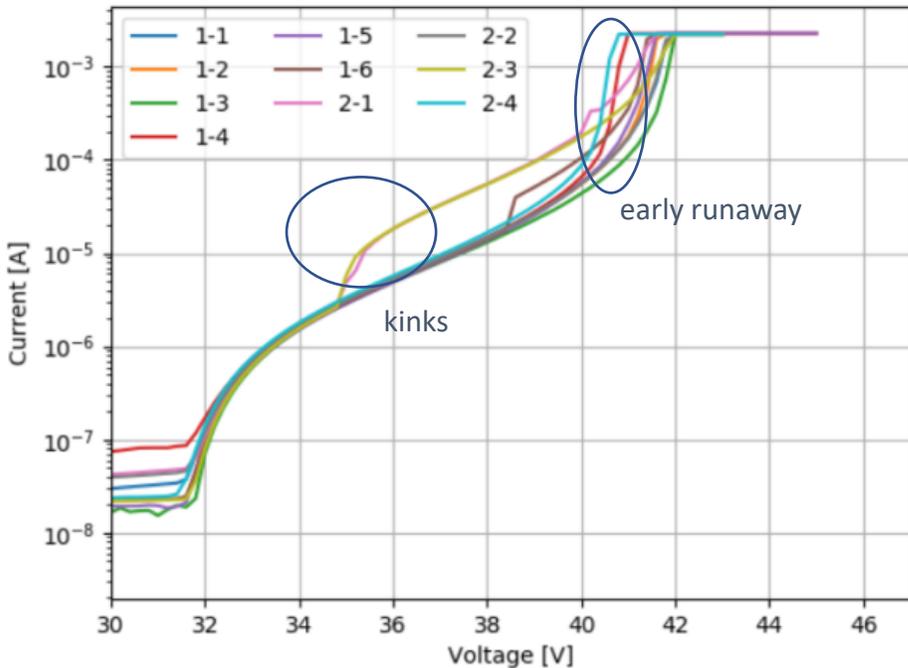


board can (welded)

4 x high density SMP feedthrough

SiPMs

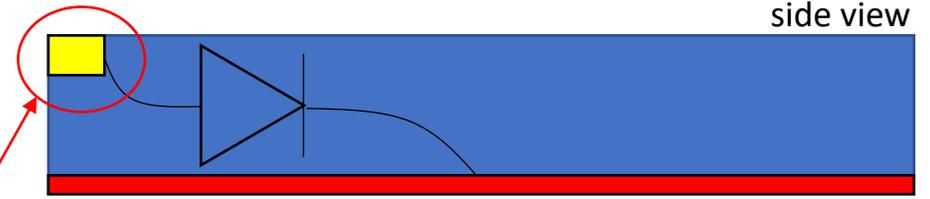
Dedicated production of VUV sensitive SiPM manufactured by FBK (1x1cm², 375mm thick)



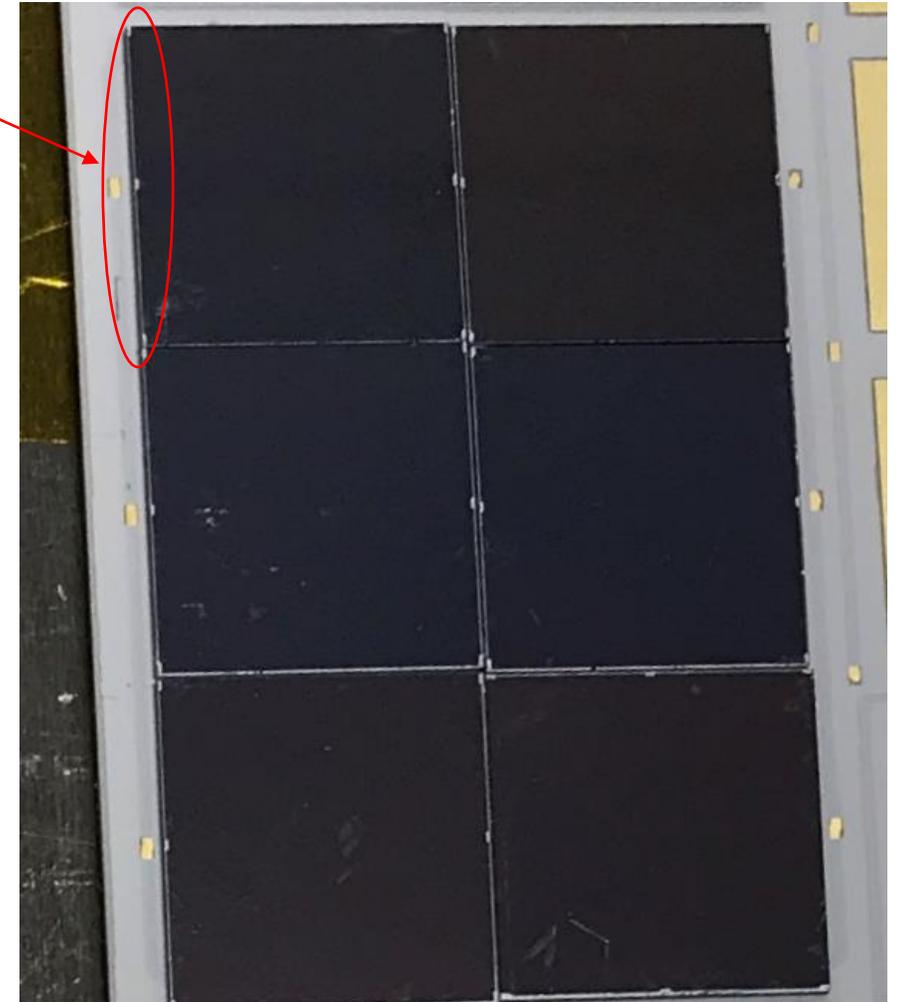
Non-uniform IV curves
across devices



Non-uniform gain for the
same voltage supplied



side view



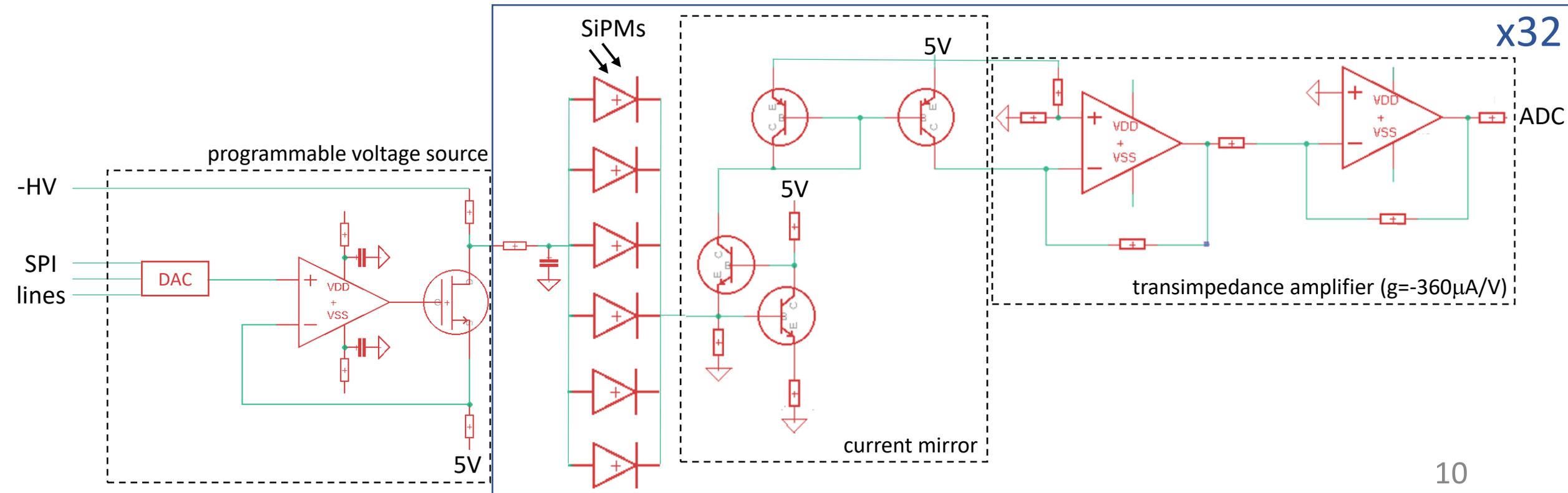
top view

anode pads

Need to supply voltage independently to each channel,
after ganging devices with similar IV curves

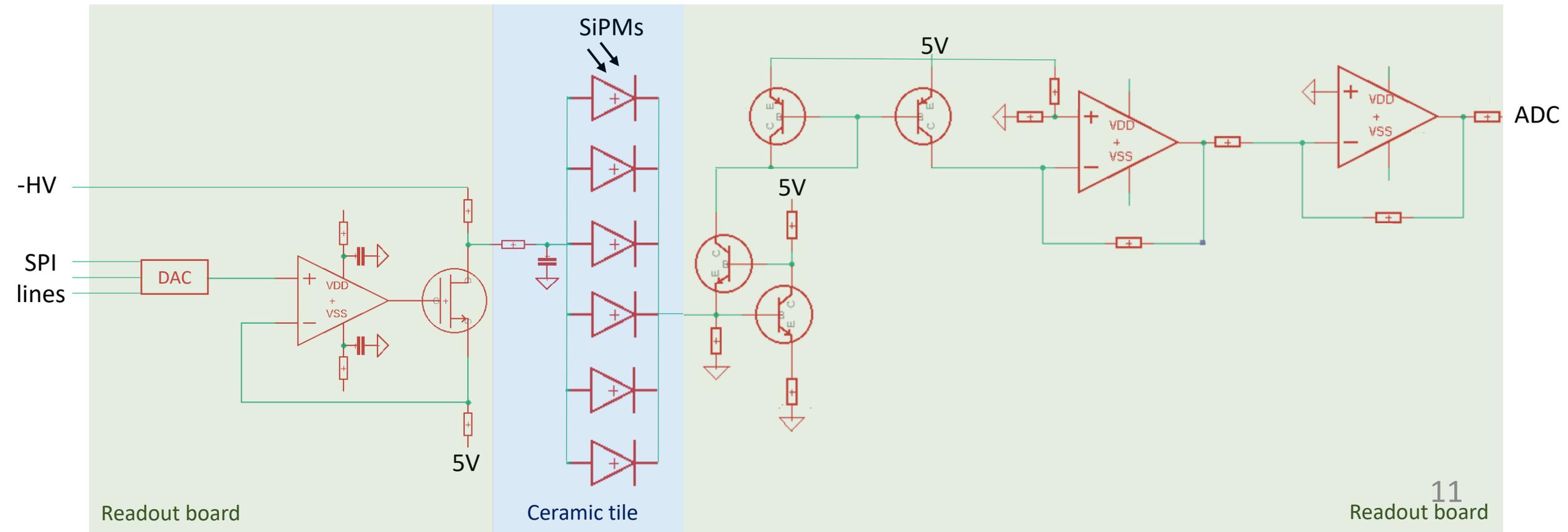
Frontend Readout

- programmable voltage to each channel (SiPMs input)
 - 4x8 channels DACs daisy-chained (SPI controlled) controlling the different biases \rightarrow only 4 wires controlling the 32 biases
- frontend amplifier for the signal (SiPMs output)
- components modularly tested at LXe temperature



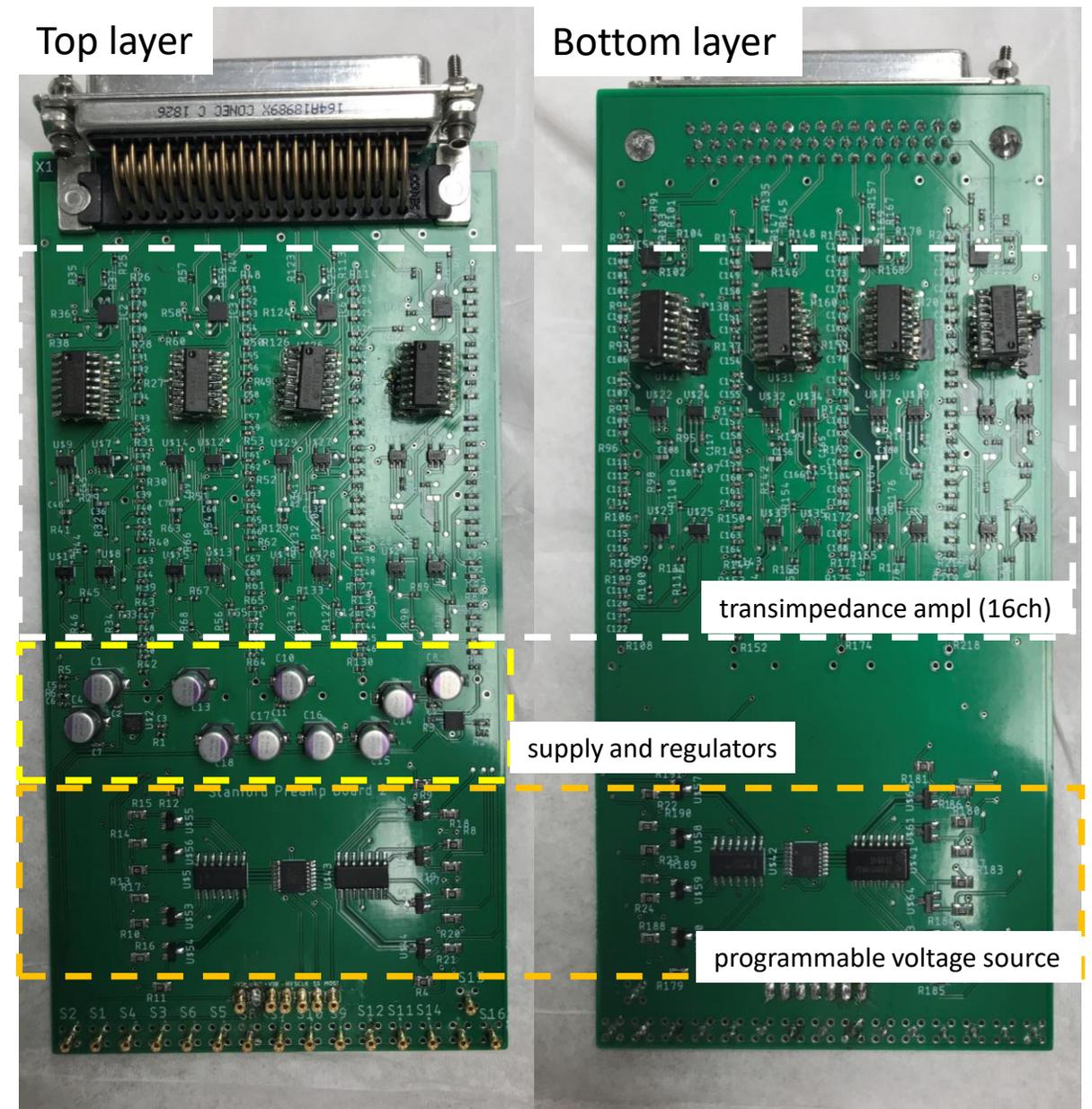
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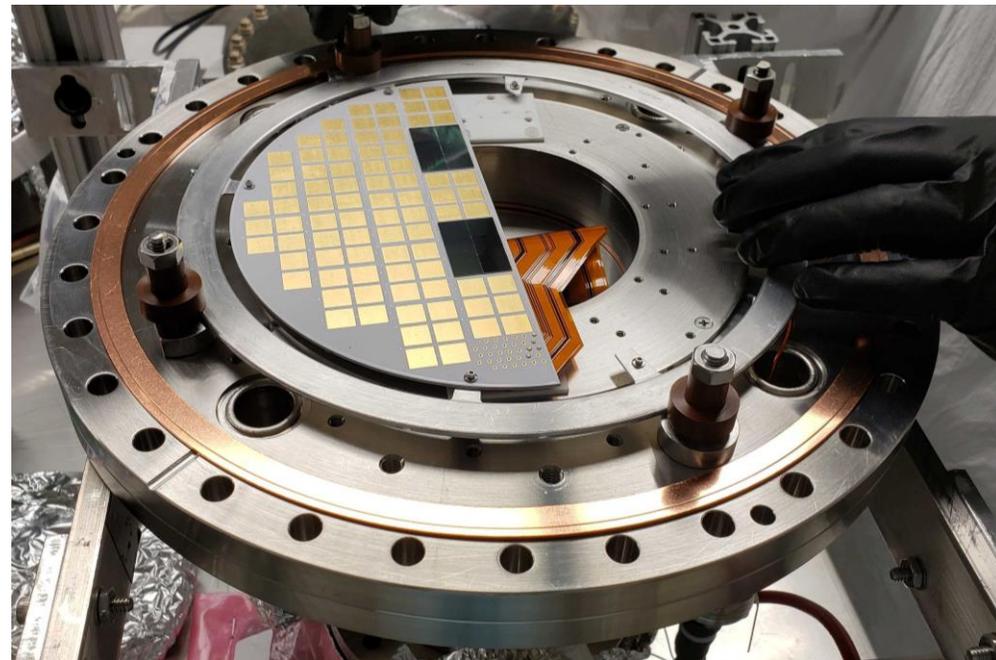
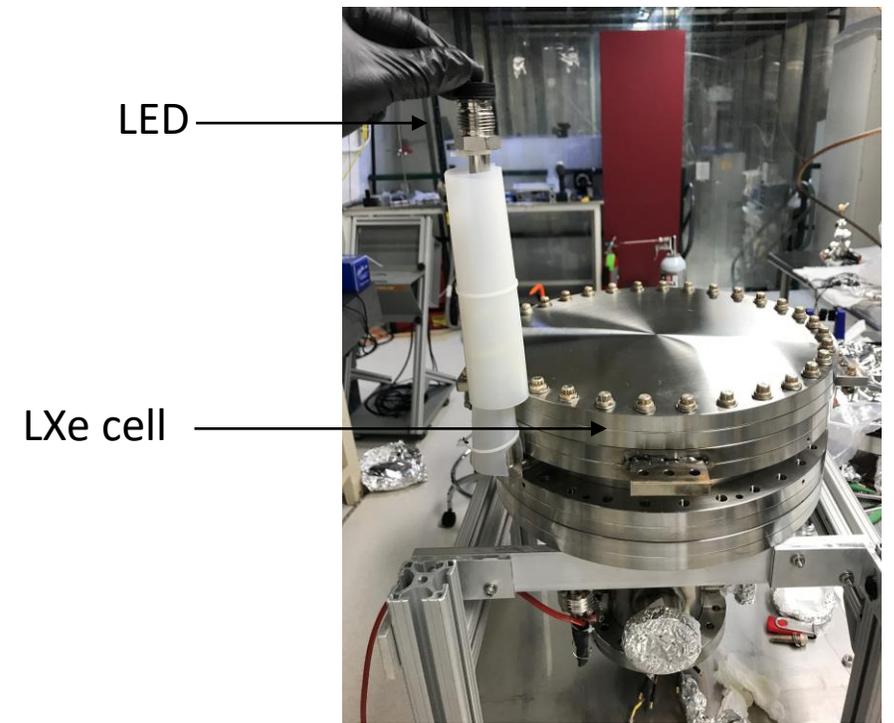
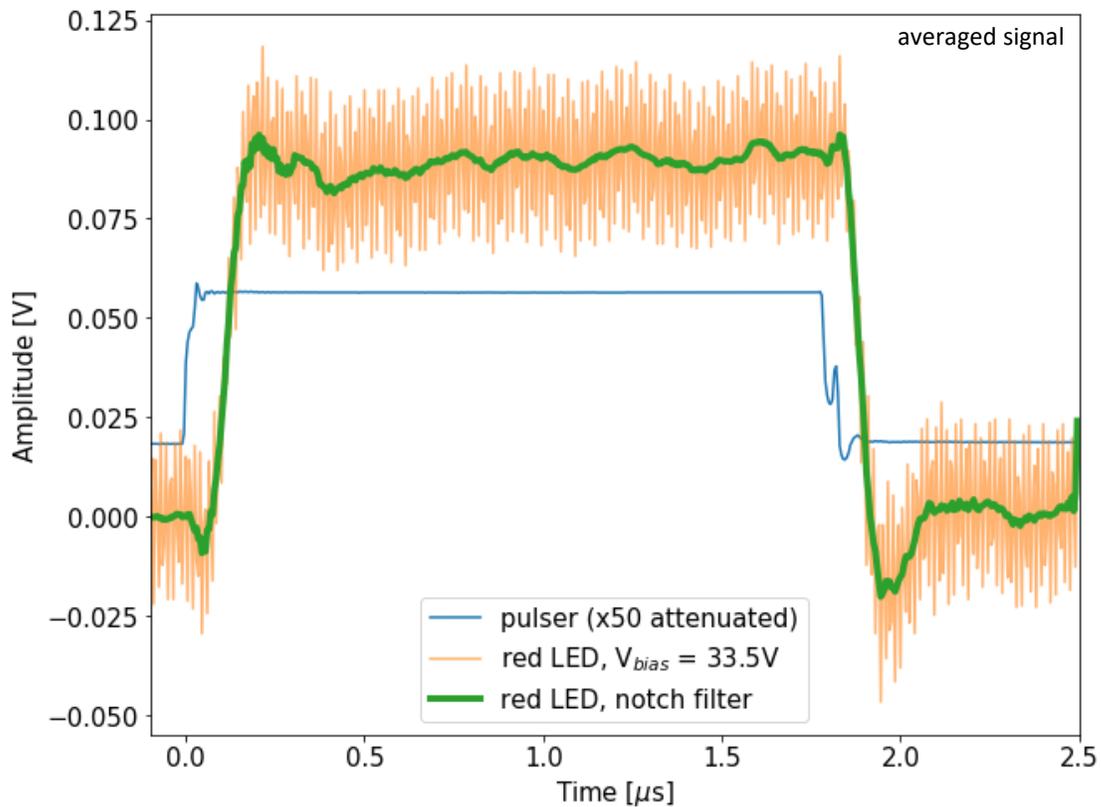


Preliminary Tests

Tile Test

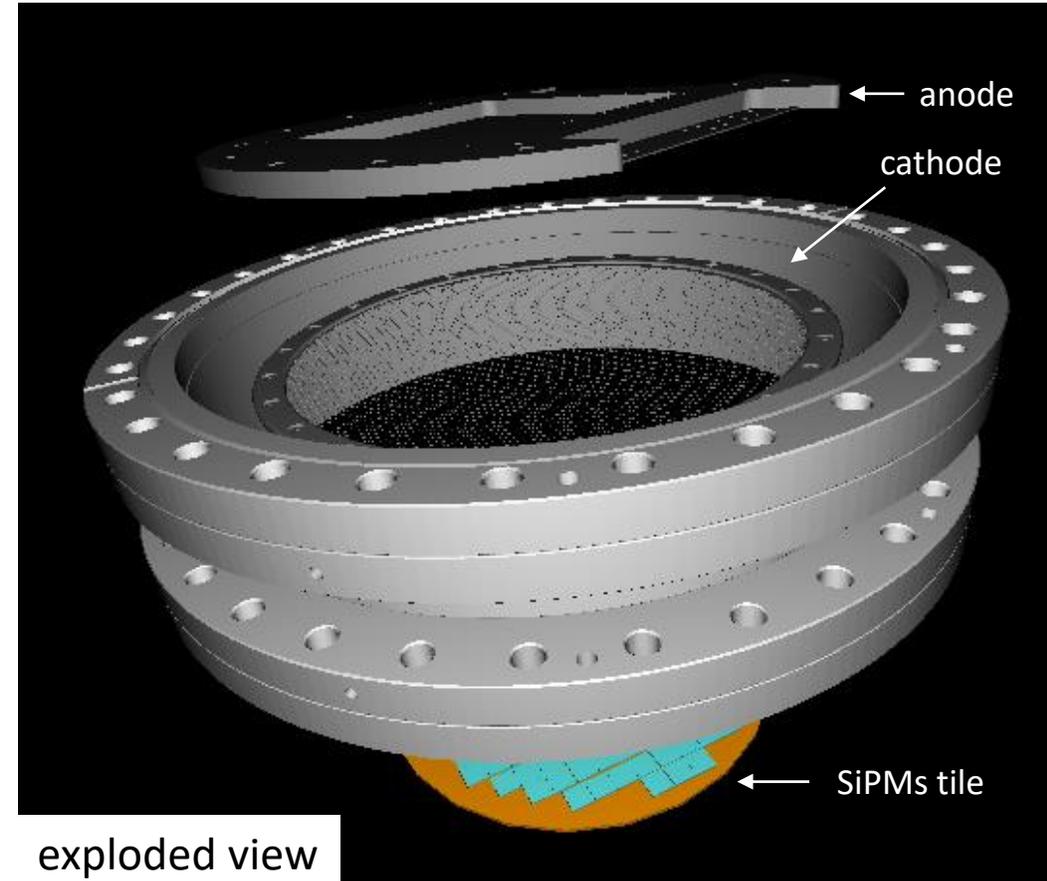
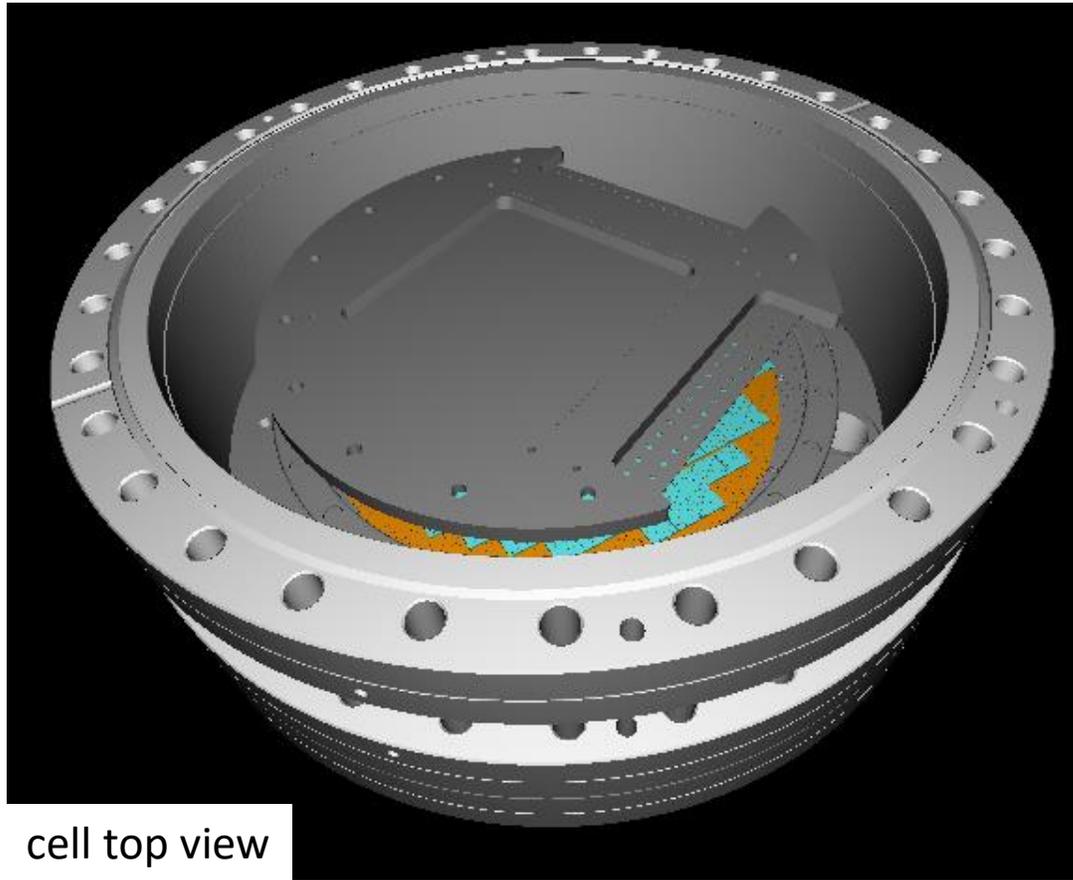
Test with pulsed LED on only one channel (2 ganged SiPMs amplified). Room temperature.

in this case C_{detector} is lower than the design one



Light Simulation

The light collection efficiency across the chamber will be also simulated with Chroma, a GPU based package for photon transport simulation.



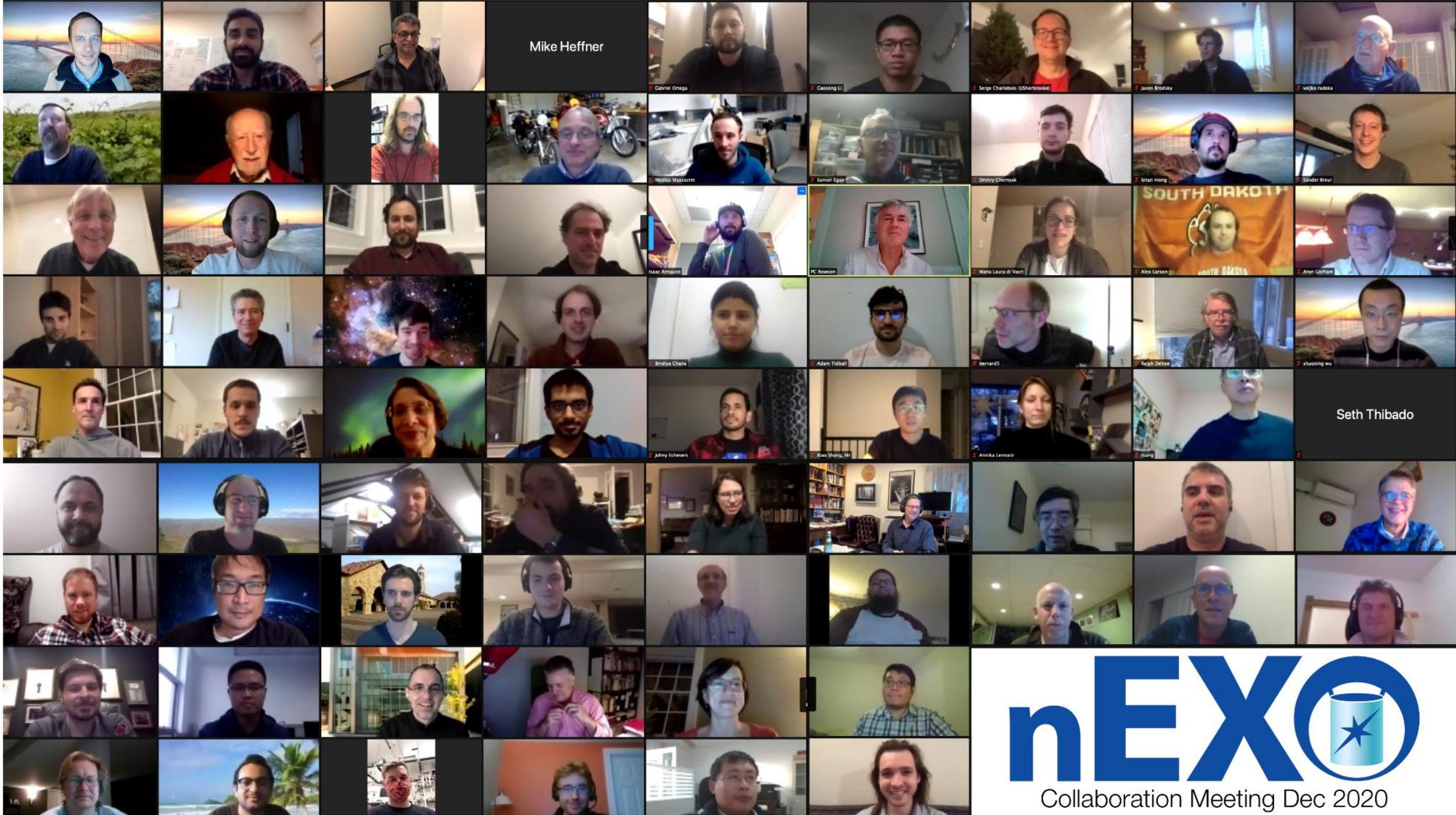
Next Steps

- A second version of the readout board is on the way (minor fixies)
- Systematic study of the oscillation, special focus on ground loops and shielding
- Full end-to-end channel test cold
- Single photon detection and dark rate measurement
- Lightmap from the simulation

Conclusion

The setup at Stanford , in phase of assembly, is one of the first large area arrays of SiPMs in LXe. The setup is tailored to study how the photon collection efficiency affects the energy resolution, useful parameter to be fed back into the light simulation, and crucial information for the nEXO final design.

After some preliminary tests, we proved that the sensors are active and, at the same time, we characterized the custom designed frontend electronics.



nEXO
Collaboration Meeting Dec 2020